Department of Computer Engineering

Computer Architecture I

Exam I

Name:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

(1) (28 pts) Answer True or False to each of the following

\_\_\_\_\_a) Processor speed increases at much faster rate than memory speed.

\_\_\_\_\_b) The C statement A = B + C; will be executed faster on RISC machine like MIPS than a CISC machine like VAX.

\_\_\_\_\_c) In The accumulator based machine an ALU operation requires only one explicit operand and also in the stack machine each memory operation requires also one explicit operand.

\_\_\_\_\_d) In mips instruction operand types is known form the operand itself.

\_\_\_\_\_e) The I-type format is used for load, store and ALU operations on immediate operands

\_\_\_\_\_f) The normalized MIPS compares machine speedup to the mips processor.

\_\_\_\_\_g) In memory alignment All addresses that start with 00 at the least two significant bits can be used to store either byte, half- word or word but not double.

(2) Short Answers

(1) (10 pts) Instruction set architecture (ISA) gives an abstraction of computer hardware design, The instruction set consists of (specify) many things name only 4 of them.

2) ( 6 pts) Name two RISC and two CISC processors

a. RISC

B. CISC

(3) (6 pts) Explain each of the following addressing modes associated with an operand address

a) memory direct

b) register (deferred)

(12 pts) Given the memory system as show below

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Address in hex | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 |
| Value in hex | AA | 88 | BB | CC | 77 | 55 | FF | BB | DD |

Show the content of $2 in hex after completing the following operations each operation is independent assume memory is big endian unless specified otherwise.

(a) Addi $4,0x50 Lh $2,2($4) \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

(b) lui $2, 0x58 ori $2,0xFFFF \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

(c) assume memory is little endian then

Lw $2, 0x54($0) \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

(d) addi $4, 0x55 Lbu $2, 2($4) \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

4) (8 pts) in mips all instruction formats are consistent with each other explain?

4. ( 30 pts) The instruction distribution of a program P which is runs on a processor X is as follows: (1) 30% of instructions are Branch, (2) 20% are Load, (3) 15% are Store, and (4) the rest are Register type. Each instruction of Branch, Load, Store, and Register takes 3 clocks, 5 clocks,4 clocks, and 2 clocks, respectively.

a. (10 pts) If the processor clock rate is 120MHZ, and program P size is 7.5 X 108 compute execution time of P on X. and the MIPS ratings of the X processor.

b. (14 pts) The processor was enhanced with respect to following issues:

• The load instruction time was reduced to 2 clocks cycles.

• The store instruction time was reduced to 3 clock cycles.

Changing cycle time to 10x10-9 seconds

Is this modification enhances the performance of the new machine if yes what is the speedup.

c (6 pts) if program p is 40% I sequential what is the maximum speedup that is ever possible for program b on any machine.