Lecture 22: Integrated circuit fabrication

Contents

1 Introduction

The starting material for integrated circuit (IC) fabrication is the single crystal silicon wafer. The end product of fabrication is functioning chips that are ready for packaging and final electrical testing before being shipped to the customer. The intermediate steps are referred to as **wafer fabrication** (including sort). *Wafer fabrication refers to the set of manufacturing processes used to create semiconductor devices and circuits.*
Some common wafer terminology used are chip, die, device, circuit, and microchip. These refer to *patterns covering the wafer surface* that provide specific functionality. The terminology *die and chip* are most commonly used and interchangeably refer to *one standalone unit on the wafer surface.* Thus, a wafer can be said to be divided into many dies or chips, as shown in figure 1.

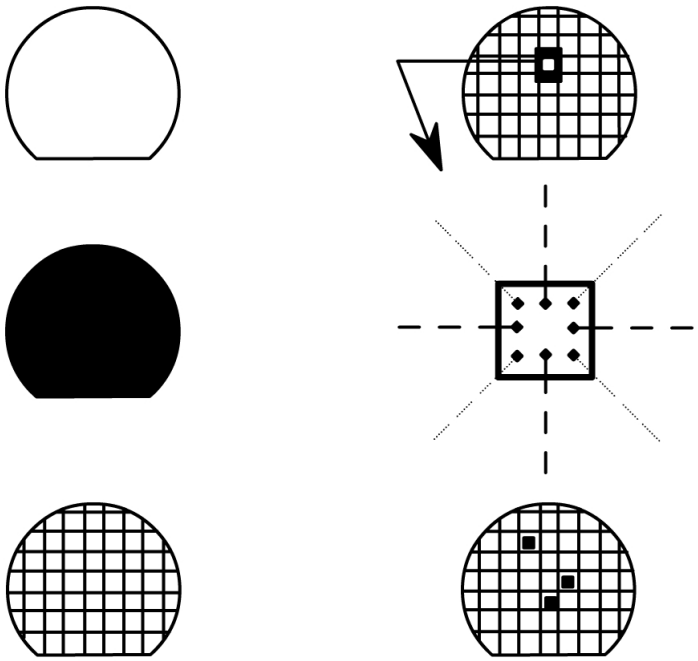

Figure 1: Schematic of wafer showing the division into individual dies. One individual die with electrical contacts is also shown. Some of these dies are used for testing. Dies at the edge dies are incomplete. Adapted from *Microchip fabrication - Peter van Zant.*

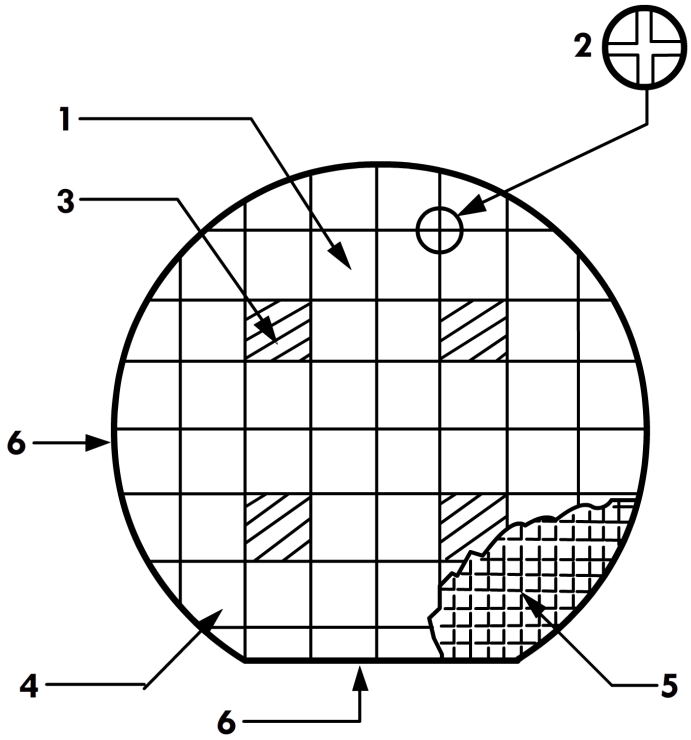

Figure 2: Schematic of various components of a wafer. (1) Chip (2) Scribe line (3) Test die (4) Edge chips (5) Wafer crystal plane (6) Flats/notches. Adapted from *Microchip fabrication - Peter van Zant.*

The area between the dies is called a **scribe line**. This is used for separating the individual dies when the fabrication is complete. Scribe lines can be blank but most often they consist of test structures that are used for electrical testing (e-test) during fabrication. This helps in identification of process issues during fabrication, without having to wait for the entire chip to be made.
Along with the regular ICs, *test dies or engineering dies* are also fabricated. These dies are used for electrical testing at the end, for process or quality control. There are also some *partial or edge dies* at the corners of the wafers. These arise because the wafers are circular while the dies are usually rectangular. Corner dies can be used for making smaller testing circuits for process control.
The various elements described above are marked in figure 2. Larger the wafer, more the number of chips that can be manufactured (including edge chips). Consider the Intel *i7* core processor (codename Ivybridge) with a die

area of 160 mm^2. For 300 mm wafers, this translates to a total of 440 dies (including edge chips), while with 450 mm wafers, the total number of dies are 994 (area of wafer by area of die calculation). To exclude edge chips, we can take the die to be a square. This gives 281 dies for 300 mm wafers and 633 dies for the larger 450 mm wafers. Thus, it is more economical to manufacture on larger wafers, but there will be initial tool costs associated with larger wafers.
There are a number of different steps in IC fabrication. Typically, a wafer can moves from one processing step to another, similar to an *assembly line manufacturing*. There are also inspection steps in the process flow to check for quality. There are different schemes for classifying the processing steps in IC fabrication. In one such scheme, the basic fab operations (processing steps) are divided into four main categories.

1. Layering
2. Patterning
3. Doping
4. Heat treatment

2 Layering

The layering step is used to *add thin layers* to the wafer surface. These layers can be of a different material or a different microstructure or composition of the same material (polycrystalline Si or silicon oxide). Figure 3 shows the cross-section of a simple MOSFET, highlighting the various thin layers that are part of the device. The different layers help in defining the various components of the MOSFET and in obtaining a functional device e.g. the passivation layer helps in electrically isolating the metal contacts to the source, drain and gate. Layering can be of many different types, though they can be broadly classified into two main categories: **grown and deposited**. The various types of layering operations are shown in figure 4.

In the case of grown layers, the underlying wafer material (typically Si) is consumed. A classic example is the growth of the oxide layer, as shown in the MOSFET structure in figure 3. This is formed by oxidation of Si into SiO_2 and is usually done in two ways.

$$\begin{aligned} \text{Dry ox}: \; Si\,(s) \; + \; O_2\,(g) \; &\rightarrow \; SiO_2\,(s) \\ \text{Wet ox}: \; Si\,(s) \; + \; H_2O\,(g) \; &\rightarrow \; SiO_2\,(s) \; + \; 2H_2\,(g) \end{aligned} \tag{1}$$

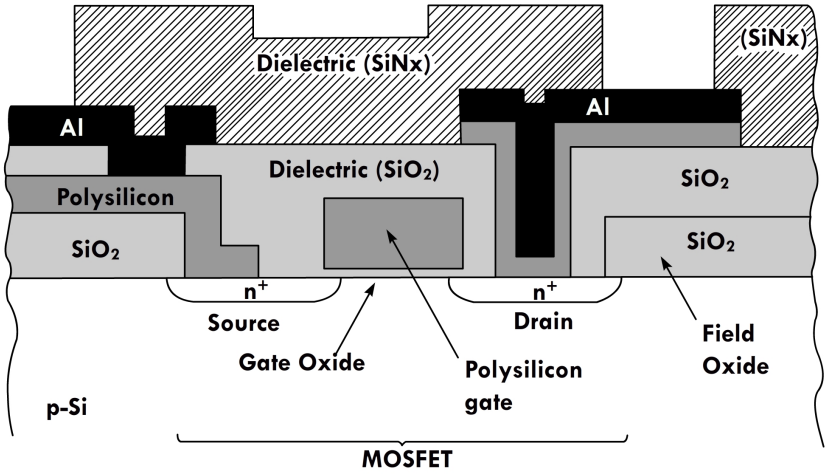

Figure 3: Cross section of a MOSFET showing the different layers. Poly Si is used as gate with SiN_x used as the interlayer dielectric. Layering is the process by which all of these different materials are added to the MOSFET. Adapted from *Fundamentals of semiconductor manufacturing and process control - May and Spanos.*

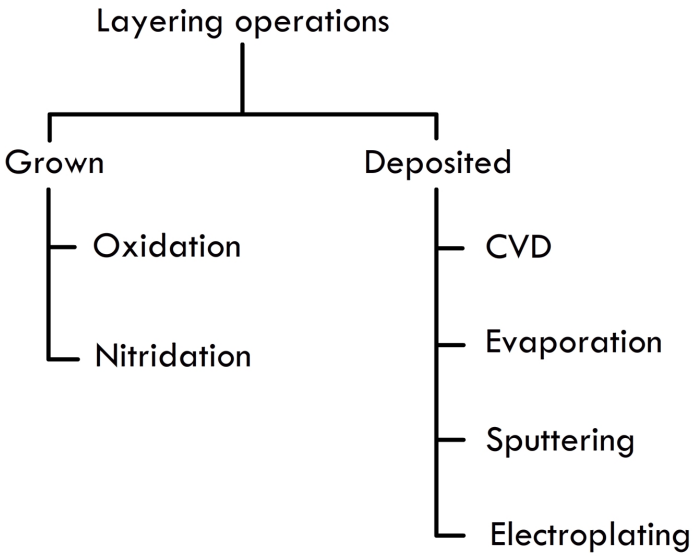

Figure 4: Different kinds of layering steps. All layering steps are classified into two major types. Grown layers use the underlying silicon substrate to form new layers. Deposited layers do not consume the silicon but are added to the surface. Adapted from *Microchip fabrication - Peter van Zant.*

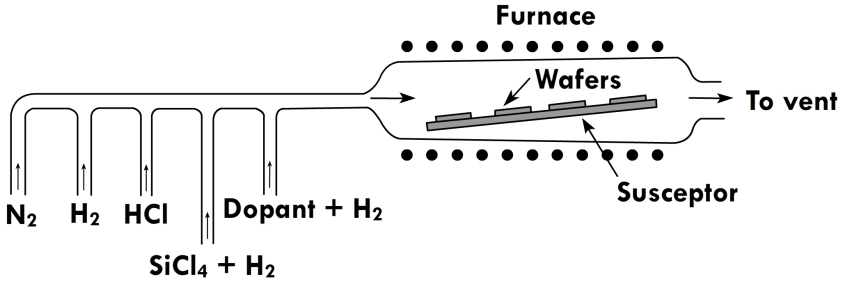

Figure 5: CVD process for growth of Si. Polycrystalline Si is formed by reduction of tetra chlorosilane by H_2, which is deposited on the wafers. The poly Si can be doped and is used as gate for the MOSFET. Adapted from *Fundamentals of semiconductor manufacturing and process control - May and Spanos.*

In both cases, the SiO_2 layer is formed on the surface by consuming the underlying Si layer. For further oxidation, the oxidizing species (O_2 or H_2O) has to diffuse through the oxide to reach the Si surface. Similarly, nitrides can also be grown by consumption of Si.
In the case of deposited films, the underlying Si is not consumed but a new layer is added on top. An example of this is the growth of epitaxial layers by a chemical vapor deposition (CVD) process. The epitaxial layer grown can be the same material as the substrate (*homoepitaxy*) or can be a different material (*heteroepitaxy*). Si can be grown epitaxially on Si wafers by reduction of tetra chlorosilane.

$$SiCl_4\,(g)\ +\ 2H_2\,(g)\ \rightarrow\ Si\,(s)\ +\ 4HCl\,(g) \tag{2}$$

The process is shown in figure 5. The chemical reaction in CVD takes places in the vapor phase. It is very useful for growing high aspect ratio structures like trenches, where CVD provides conformal coatings. Figure 6 shows an exzmple of CVD growth of CrB_2 on deep trenches by CVD.
Molecular beam epitaxy (MBE) is another growth technique where the constituents of the epitaxial layer are evaporated from separate sources ('molecular beam') and then combine on the substrate to form the epitaxial layer. It is also possible to introduce dopants in this process by evaporating the dopant material separately. GaAs can be grown by MBE by evaporating from Ga and As sources. To dope this *p*-type, Be can also be evaporated in the required concentration along with Ga and As.
Thermal evaporation and sputtering are other examples of layering operations. These fall under *physical vapor deposition techniques* where the material, in the final form, is deposited onto the wafer. This can be used for

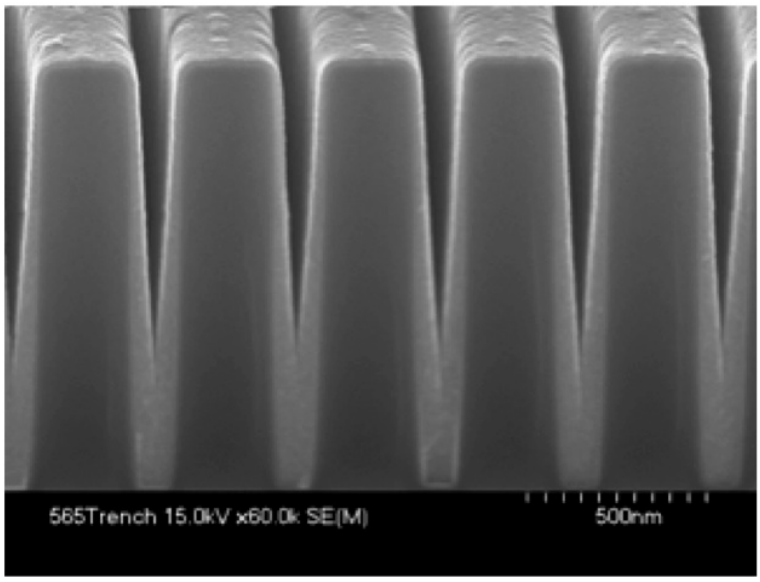

Figure 6: Chromium boride coatings grown by CVD in deep trenches. The coatings are highly conformal to the trench dimensions. This cannot be achieved by other deposition techniques since the opening will be filled up before depositing in the trench. Source *http://abelson.matse.illinois.edu/*

metals, oxides, nitrides, and other types of layers. Electroplating is another layering operation. This is mainly used for depositing copper, which is used as interconnects in the IC.

3 Patterning

Patterning or lithography is one of the most important steps in wafer fabrication. Patterning refers to a series of steps to *selectively mask or expose* portions of the surface for deposition/doping/etching. It sets the *critical dimensions* of the device. The drive to pack more devices in a chip (smaller devices) is directly related to the ability to pattern smaller regions in the wafer. The challenges in reduction of device size in recent ICs is related to patterning. The process is highly defect sensitive, especially at smaller sizes, as shown in figure 7. Presence of defect particles in the pattern can affect the later steps like deposition/doping/etching and can also affect pattering of other layers.
To make a pattern, *reticle* has to be first prepared. Reticle refers to the hard copy of the design that is then transferred on to the chip. This hard copy

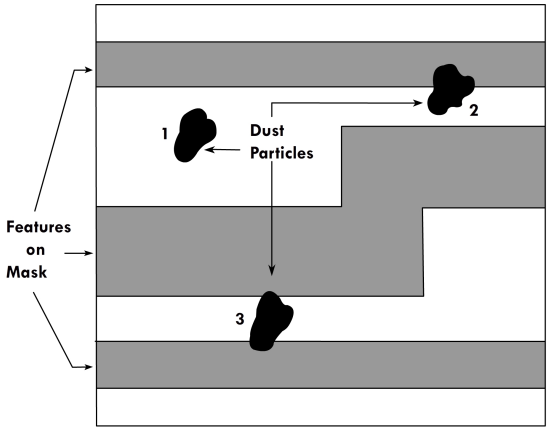

Figure 7: Effect of defect particles on patterning process. Defects that cause damage to the ICs are called *killer defects*. Not all defects are killer defects, but with reduction in size, more defects can turn into killer defects. Adapted from *Fundamentals of semiconductor manufacturing and process control - May and Spanos.*

is generated by 'writing' the pattern, using a laser beam or electron beam, and is usually done on chrome coated glass. The design is then copied on to the chip using a suitable photoresist and UV exposure. The pattern transfer can be $1:1$ or the size can be reduced by a suitable lens system. Either the pattern or its negative can be transferred by suitable choice of photoresist and the process is summarized in figure 8.

Use of photoresists for patterning is an example of a *soft mask* since the mask can be easily removed without damaging the underlying substrate. Sometimes oxide or nitride layers are also used as masks for pattern transfer. These are called *hard masks*, since these masks can withstand high temperature while resists cannot and they also need aggressive chemical procedures for removal. Thus, it is difficult to combine lithography with deposition processes like CVD (where hard mask would be needed) but it can be used with processes like thermal evaporation, sputtering, and e-beam deposition.

4 Doping

Doping refers to the process where *specific amounts* of electrically active 'impurities' are incorporated through openings on the wafer surface. The dopant materials are typically p or n type impurities and they are needed to form devices like diodes, transistors, conductors, and other electronic devices

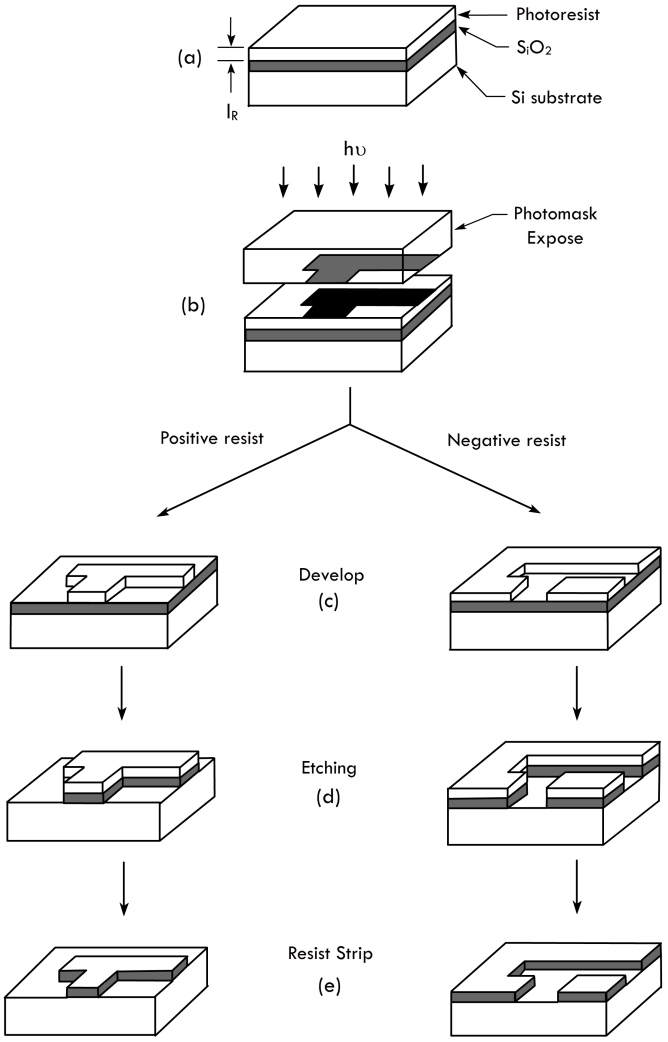

Figure 8: Overview of the patterning process, showing both positive and negative photoresists. Positive resists directly transfer the pattern from reticle to wafer, while negative resists transfer the inverse of the pattern. Adapted from *Fundamentals of semiconductor manufacturing and process control - May and Spanos.*

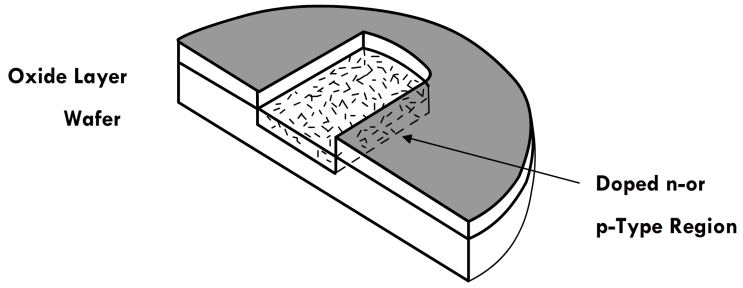

Figure 9: p or n type doped region in a wafer. An oxide layer is used as a hard mask to control the region where doping occurs. Adapted from *Microchip fabrication - Peter van Zant.*

that combine to form the IC. Typical p type impurities, for Si, include B while n type impurities can be As, P, or Sb. The formation of a doped region in a section of the wafer is shown in figure 9. There are two main techniques for doping

1. Thermal diffusion
2. Ion implantation

Both processes produce different dopant concentration profiles at and below the surface, as shown in figure 10.

4.1 Thermal diffusion

As the name implies, in thermal diffusion, doping is carried out by movement of the dopant material from the surface to the bulk, by a thermally activated process. The diffusion can be initiated from dopants in a vapor, liquid, or a solid source. The wafer has to be heated to high temperature, around 1000 °C, to speed up the diffusion process. Thus, thermal diffusion cannot be used with soft lithography masks and a hard mask like oxide or nitride is used. For n type doping in Si, some typical dopant materials are Sb_2O_3 (s), As_2O_3 (s), AsH_3 (g), $POCl_3$ (l), P_2O_5 (s), and PH_3 (g). For p type doping, typical materials are BBr_3 (l), B_2O_3 (s) and BCl_3 (g). Thermal diffusion is an isotropic process (though diffusion rates might be different in different directions). This leads to lateral spread of the dopants, as seen in figure 10, at higher temperatures and long times, and makes doping in small confined regions difficult. Also, the high temperature means that thermal diffusion

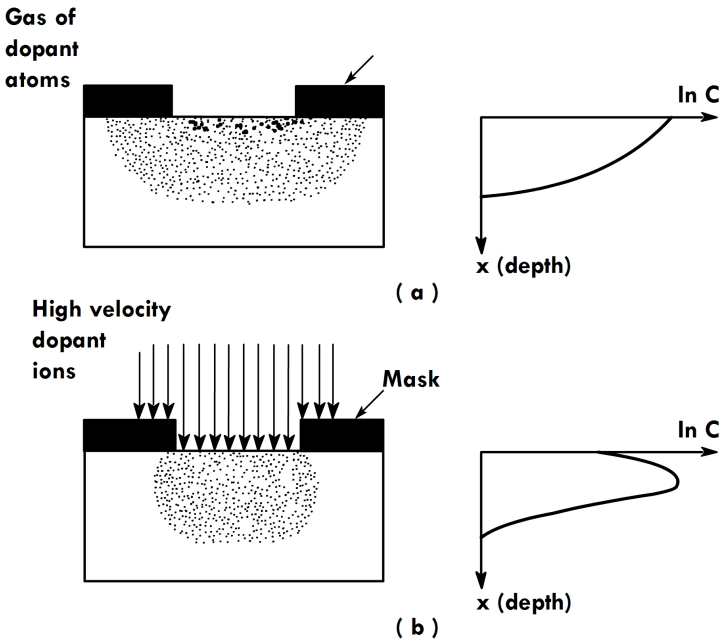

Figure 10: Schematic of the doping process and concentration profiles in (a) thermal diffusion and (b) ion implantation. In thermal diffusion, the highest concentration is at the surface while for ion implantation, the highest concentration is below the surface. Adapted from *Fundamentals of semiconductor manufacturing and process control - May and Spanos.*

cannot be used in the later stages of the fabrication process, since there could be a number of layers that might not be able to withstand the high temperature.

4.2 Ion implantation

For doping in specific regions, ion implantation is used. Here, the dopant atoms are ionized and then made to impinge on the wafer surface where they penetrate and get 'implanted' into the wafer. The advantage of this process is that doping can be done at room temperature so that soft masks can be used. This also enables doping in small regions since lateral diffusion is minimized. Ion implantation causes beam damage so there is a rapid annealing treatment post implantation to repair the wafer and 'activate' the dopants.

5 Heat treatment

Heat treatment operations are usually part of the other three operations i.e. layering, doping, and patterning. Some of the heat treatment operations in these steps are summarized in table 1.

Table 1: Heat treatment operations in IC fabrication. The link with other fabrication steps is tabulated.

Operation	**Heat treatment**
Patterning	Soft bake Hard bake Post exposure bake develop
Doping	Post ion implant anneal
Layering	Post metal deposition and patterning anneal

6 MOSFET fabrication

Consider the fabrication of a Si MOSFET device as an example to illustrate the various types of fab processes. The various steps in fabricating the device, starting from the bare wafer, are shown in figure 11. The process goes through various steps which fall under the categories listed above. Starting from the bare wafer, the various steps to get the finished MOSFET are listed below. The individual stages can be followed using figure 11.

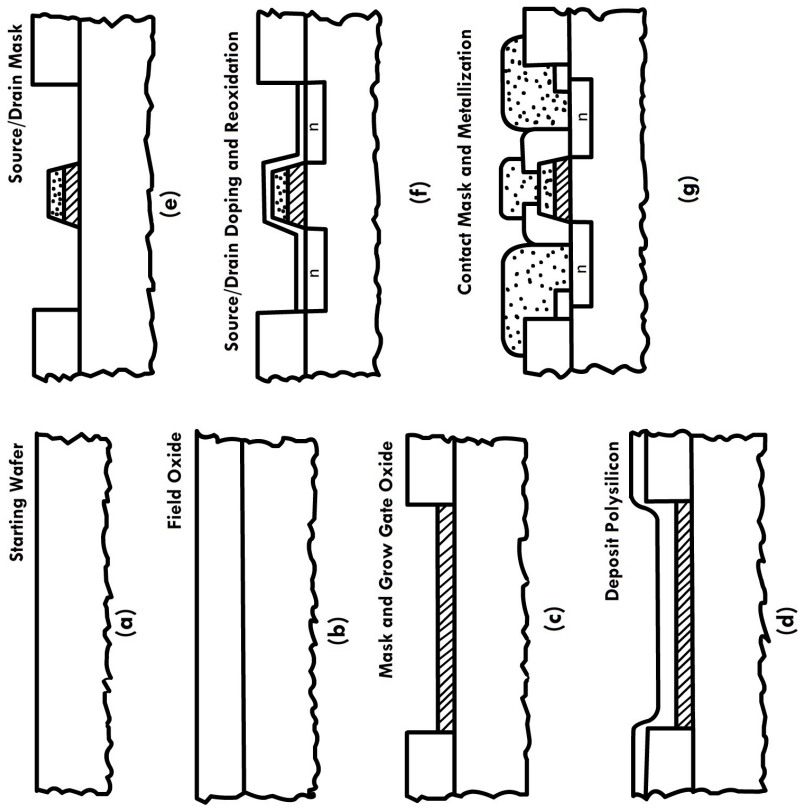

Figure 11: An overview showing the various steps in MOSFET fabrication. (a) Staring wafer is (b) oxidized and then (c) patterned to grow the field oxide. (d) Poly Si is then deposited and (e) patterned to form the gate on top of the oxide. (f) A further patterning and doping is done to define the source and drain and (g) finally metallization is done to define the contacts. Adapted from *Microchip fabrication - Peter van Zant.*

1. **Layering** - the first step is the growth of an oxide layer (field oxide). This is used as hard mask for patterning.

2. **Patterning** - next an opening is created in the field oxide for growing source, drain and the gate oxide. Patterning refers to the series of steps that create this opening in the oxide.

3. **Layering** - the field oxide is removed (etched) and then the gate oxide is grown. In early MOSFETs, this was just SiO_2, but later devices use oxy nitrides and high-k dielectrics.

4. **Layering** - a layer of poly-Si is deposited on top of the gate oxide. This forms the gate electrode. Typically poly Si is grown by a CVD process. Initially, the poly Si is deposited uniformly.

5. **Patterning** - two openings are then created in the gate oxide layer. This is for making the source and drain. The gate region is masked and the material (poly Si and SiO_2) in the remaining regions are removed by a process called etching (opposite of layering).

6. **Doping** - doping is used to create the n regions (source and drain). This is when the base Si is a p-type Si.

7. **Layering** - an uniform oxide layer is now grown on top. This will be used to insulate the source, drain, and gate, when electrical contacts are made.

8. **Patterning** - openings are created in the oxide layer for making the electrical contacts. The remaining oxide layer helps in electrical insulation.

9. **Layering** - metal is deposited to make the electrical contacts. In the earlier MOSFETs, Al was the metal of choice though now Cu is used with a suitable barrier layer, typically tungsten nitride or silicide.

10. **Patterning** - the excess metal is removed from the device.

11. **Heat treatment** - the MOSFET is annealed so that better electrical contacts can be made. In some cases the Si reacts with the metal to form silicides, which form Ohmic contacts with Si.

12. **Layering** - oxide layers are grown on top to form a passivation layer. This also acts as a protection layer for the device.

13. **Patterning** - the last step is a patterning step to creates holes in the passivation layer for the electrical contacts to the external circuits. This step and the one above it are not shown in figure 11.

This 13-step process illustrates the various steps to make a MOSFET from Si. Similarly, there are steps for making other device components. All of these are integrated to make the final IC circuit. Along with processing, there are inspection steps at various stages and electrical testing at the end. This is to make sure that device specifications are correctly implemented. This includes the physical dimensions of the various components (width and height) and the electrical properties (I-V characteristics).