Lecture 21: Silicon wafer manufacturing

Contents

1 Introduction

The first step in integrated circuit (IC) fabrication is preparing the high purity single crystal Si wafer. This is the starting input to the fab. Typically, *Si wafer* refers to a single crystal of Si with a *specific orientation, dopant type, and resistivity* (determined by dopant concentration). Typically, Si (100) or Si (111) wafers are used. The numbers (100) and (111) refers to the orientation of the plane parallel to the surface. The wafer should have structural defects, like dislocations, below a certain permissible level and impurity (undesired) concentration of the order of *ppb* (parts per billion).
Consider the *specs* (specifications) of a 300 mm wafer shown in table 1 below. The thickness of the wafer is less than 1 mm, while its diameter is 300 mm. Also, the wafers must have the 100 plane parallel to the surface, to within 2$\circ$ deviation, and typical impurity levels should be of the order of *ppm* or less with metallic impurities of the order of *ppb*. For doped wafers, there should be specific amounts of the desired dopants (p or n type) to get the required resistivity.

Table 1: Specs of a typical 300 mm wafer used in fabrication. The specifications include the dimensions, orientation, resistivity, and oxygen and carbon impurity content.

Specs	**Value**
Diameter	300 ± 0.02 mm
Thickness	$775 \pm 25\ \mu m$
Orientation	$100 \pm 2^{\circ}$
Resistivity	$> 1\ \Omega - m$
Oxygen concentration	20-30 ppm
Carbon concentration	< 0.2 ppm

Table 2: Impurities in MGS, after the submerged arc electrode process.

Element	**Concentration** (ppm)
Al	1000-4350
B	40-60
Ca	245-500
Fe	1550-6500
P	20-50
Cu	15-45

2 Poly Si manufacture

The starting material for Si wafer manufacture is called *Electronic grade Si* (EGS). This is an ingot of Si that can be shaped and cut into the final wafers. EGS should have impurity levels of the order of *ppb*, with the desired doping levels, so that it matches the chemical composition of the final Si wafers. The doping levels are usually back calculated from resistivity measurements. To get EGS, the starting material is called *Metallurgical grade Si* (MGS). The first step is the synthesis of MGS from the ore.

The starting material for Si manufacture is *quartzite* (SiO_2) or *sand*. The ore is reduced to Si by mixing with coke and heating in a submerged electrode arc furnace. The SiO_2 reacts with excess C to first form SiC. At high temperature, the SiC reduces SiO_2 to form Si. The overall reaction is given by

$$SiC\ (s)\ +\ SiO_2\ (s)\ \rightarrow\ Si\ (l)\ +\ SiO\ (g)\ +\ CO\ (g) \tag{1}$$

The $Si(l)$ formed is removed from the bottom of the furnace. This is the MGS and is around 98% pure. The schematic of the reducing process is shown in figure 1. Typical impurities and their concentrations in MGS is tabulated in 2. MGS is used for making alloys. From table 2 it can be seen that the main

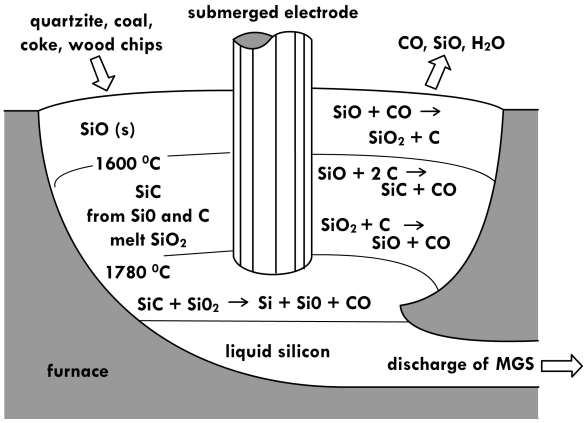

Figure 1: Schematic of the submerged arc electrode process. SiO_2 is mixed with coke and heated. It first forms SiC, which further reacts with the remaining SiO_2 forming silicon. The temperature is maintained above the melting point of silicon so that the molten semiconductor is removed from the bottom. Adapted from *Synthesis and purification of bulk semiconductors - Barron and Smith*

metallic impurities are Al and Fe. Further purification is needed to make EGS since the impurity concentration must be reduced to *ppb* levels.
One of the techniques for converting MGS to EGS is called the **Seimens process**. In this the Si is reacted with HCl gas to form tricholorosilane, which is in gaseous form.

$$Si\ (s)\ +\ 3HCl\ (g)\ \rightarrow\ SiHCl_3\ (g)\ +\ H_2\ (g) \tag{2}$$

This process is carried out in a *fluidized bed reactor* at 300°C, where the trichlorosilane gas is removed and then reduced using H_2 gas.

$$2SiHCl_3\ (g)\ +\ 2H_2\ (g)\ \rightarrow\ 2Si\ (s)\ +\ 6HCl\ (g) \tag{3}$$

The process flow is shown in figure 2. A Si rod is used to nucleate the reduced Si obtained from the silane gas, as shown in figure 3. During the conversion of silicon to trichlorosilane impurities are removed and process can be cycled to increase purity of the formed Si. The final material obtained is the EGS. This is a polycrystalline form of Si, like MGS, but has much smaller impurity levels, closer to what is desired in the final single crystal wafer. The impurities in EGS are tabulated in 3. EGS is still polycrystalline and needs to be converted into a single crystal Si ingot for producing the wafers.

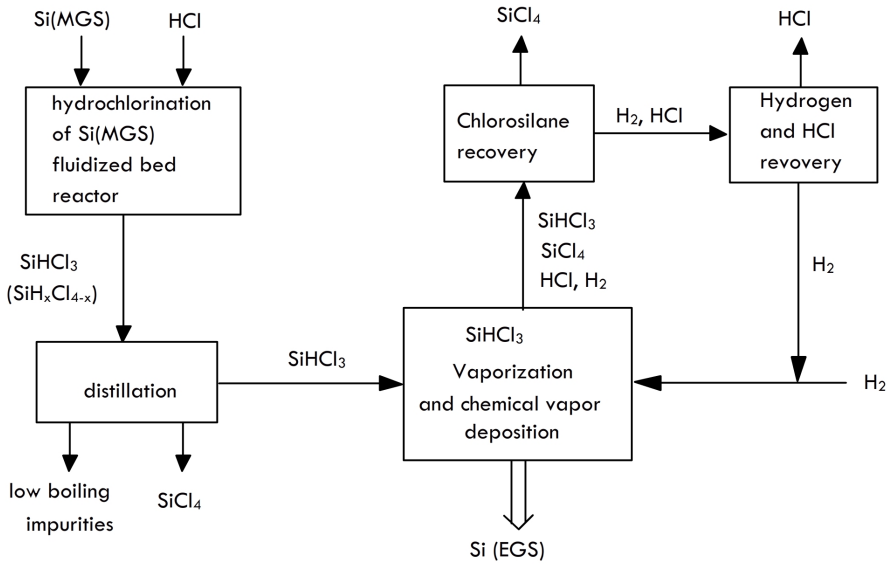

Figure 2: Schematic of the process to purify MGS to obtain EGS. The process involves conversion of silicon to trichlorosilane gas, which is purified, and then reduced to obtain silicon. Adapted from *Synthesis and purification of bulk semiconductors - Barron and Smith*

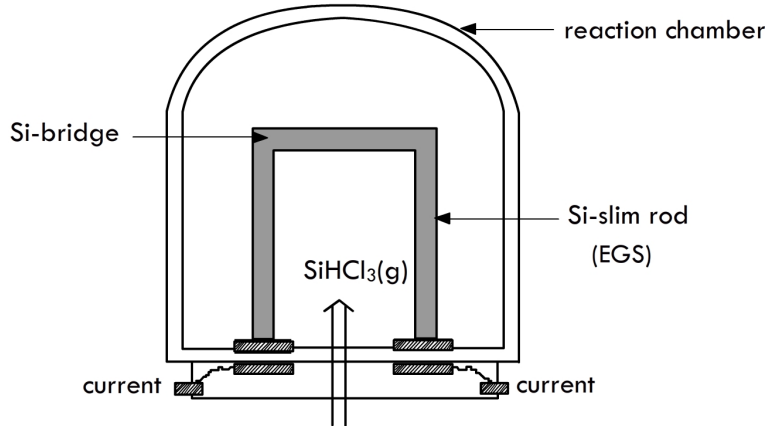

Figure 3: The Seimens deposition reactor where the purified Si is condensed. This is the electronic grade Si, same purity level as Si wafers, but polycrystalline. Adapted from *Synthesis and purification of bulk semiconductors - Barron and Smith*

Table 3: Impurities in EGS, after purification from MGS. Compared to table 2, the concentration levels of the metals have dropped to *ppb* levels.

Element	**Concentration** (*ppb*)
As	<0.001
Sb	<0.001
B	<0.1
C	100-1000
Cu	0.1
Fe	0.1-1
O	100-400
P	<0.3

3 Single crystal Si manufacture

There are two main techniques for converting polycrystalline EGS into a single crystal ingot, which are used to obtain the final wafers.

1. **Czochralski technique (CZ)** - this is the dominant technique for manufacturing single crystals. It is especially suited for the large wafers that are currently used in IC fabrication.

2. **Float zone technique** - this is mainly used for small sized wafers. The float zone technique is used for producing specialty wafers that have low oxygen impurity concentration.

3.1 Czochralski crystal growth technique

A schematic of this growth process is shown in figure 4. The various components of the process are

1. Furnace

2. Crystal pulling mechanism

3. Ambient control - atmosphere

4. Control system

The starting material for the CZ process is electronic grade silicon, which is melted in the furnace. To minimize contamination, the crucible is made of SiO_2 or SiN_x. The drawback is that at the high temperature the inner liner of the crucible also starts melting and has to replaced periodically. The

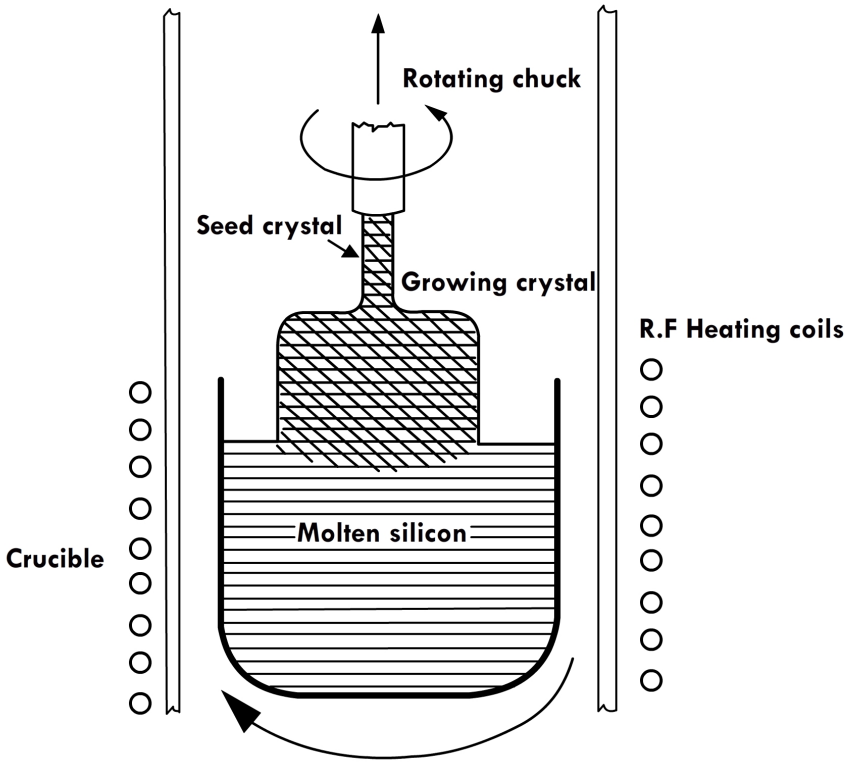

Figure 4: Schematic of the Czochralski growth technique. The polycrystalline silicon is melted and a single crystal seed is then used to nucleate a single crystal ingot. The seed crystal controls the orientation of the single crystal. Adapted from *Microchip fabrication - Peter van Zant.*

Figure 5: Single crystal Si ingot. This is further processed to get the wafers that are used for fabrication. Source *http://www.chipsetc.com/silicon-wafers.html*

furnace is heated above 1500 °C, since Si melting point is 1412 °C. A small seed crystal, with the *desired orientation of the final wafer*, is dipped in the molten Si and slowly withdrawn by the crystal pulling mechanism. The seed crystal is also rotated while it is being pulled, to ensure uniformity across the surface. The furnace is rotated in the direction opposite to the crystal puller. The molten Si sticks to the seed crystal and starts to solidify with the same orientation as the seed crystal is withdrawn. Thus, a single crystal ingot is obtained. To create doped crystals, the dopant material is added to the Si melt so that it can be incorporated in the growing crystal. The process control, i.e. speed of withdrawal and the speed of rotation of the crystal puller, is crucial to obtain a good quality single crystal. There is a feedback system that control this process. Similarly there is another ambient gas control system. The final solidified Si obtained is the single crystal ingot. A 450 mm wafer ingot can be as heavy as 800 kg. A picture of a such an ingot is show in figure 5.

3.2 Float zone technique

The float zone technique is suited for small wafer production, with low oxygen impurity. The schematic of the process is shown in figure 6. A polycrystalline EGS rod is fused with the single crystal seed of desired orientation. This is taken in an inert gas furnace and then melted along the length of the rod by a traveling radio frequency (RF) coil. The RF coil starts from the fused region, containing the seed, and travels up, as shown in figure 6. When the molten region solidifies, it has the same orientation as the seed. The furnace is filled with an inert gas like argon to reduce gaseous impurities.

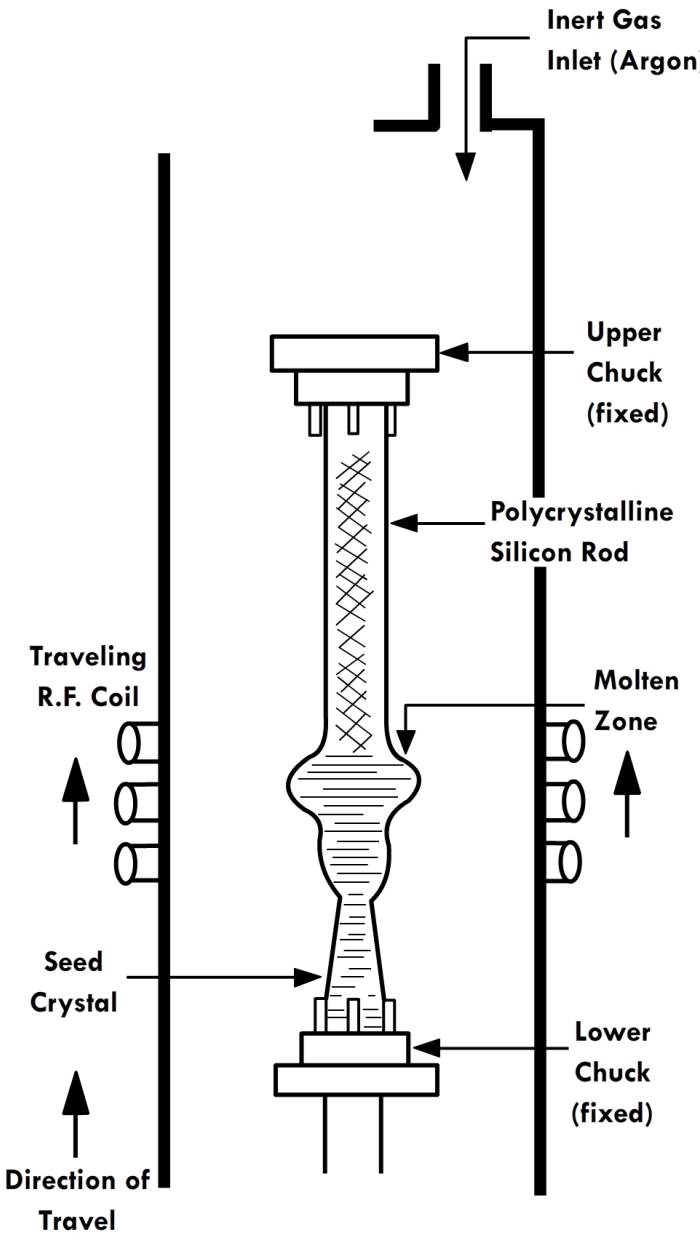

Figure 6: Schematic of the float zone technique. The polycrystalline ingot is fused with a seed crystal and locally melted by a traveling radio frequency coil. As the ingot melts and resolidifes it has the same orientation as the seed. Adapted from *Microchip fabrication - Peter van Zant.*

Also, since no crucible is needed it can be used to produce oxygen 'free' Si wafers. The difficulty is to extend this technique for large wafers, since the process produces large number of dislocations. It is used for small specialty applications requiring low oxygen content wafers.

4 Wafer manufacturing

After the single crystal is obtained, this needs to be further processed to produce the wafers. For this, the wafers need to be shaped and cut. Usually, industrial grade diamond tipped saws are used for this process. The shaping operations consist of two steps

1. The seed and tang ends of the ingot are removed.
2. The surface of the ingot is ground to get an uniform diameter across the length of the ingot.

Before further processing, the ingots are checked for resistivity and orientation. Resistivity is checked by a four point probe technique and can be used to confirm the dopant concentration. This is usually done along the length of the ingot to ensure uniformity. Orientation is measured by x-ray diffraction at the ends (after grinding).
After the orientation and resistivity checks, one or more *flats* are ground along the length of the ingot. There are two types of flats.

1. **Primary flat** - this is ground relative to a specific crystal direction. This acts as a visual reference to the orientation of the wafer.
2. **Secondary flat** - this used for identification of the wafer, dopant type and orientation.

The different flat locations are shown in figure 7. p-type (111) Si has only one flat (primary flat) while all other wafer types have two flats (with different orientations of the secondary flats). The primary flat is typically longer than the secondary flat. Consider some typical specs of 150 mm wafers, shown in table 4. Bow refers to the flatness of the wafer while Δt refers to the thickness variation across the wafer.
After making the flats, the individual wafers are sliced per the required thickness. *Inner diameter (ID) slicing* is the most commonly used technique. The cutting edge is located on the inside of the blade, as seen in figure 8. Larger wafers are usually thicker, for mechanical integrity.
After cutting, the wafers are chemically etched to remove any damaged and

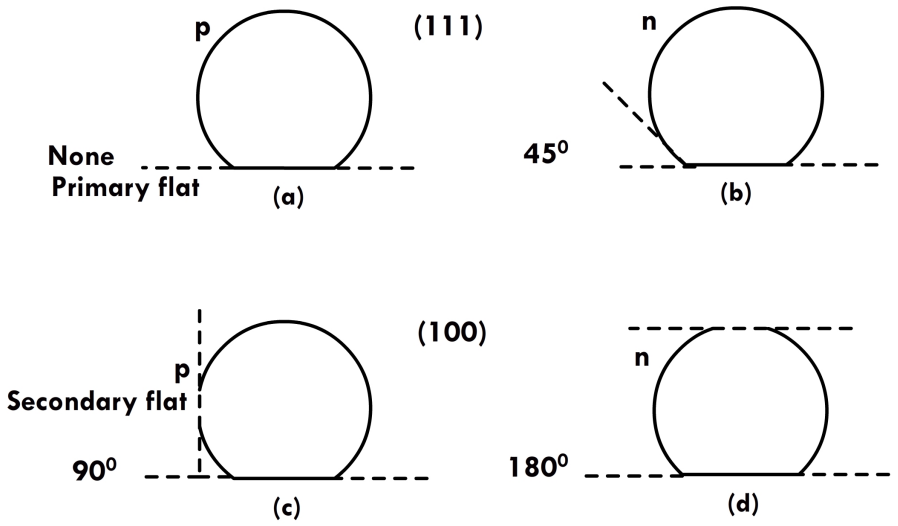

Figure 7: Flats for the different wafer types and orientations. All orientations and doping types have a primary flat, while there are different secondary flats for different types (a) p(111) (b) n(111) (c) p(100) and (d) n(100). Adapted from *Microchip fabrication - Peter van Zant.*

Table 4: Specs of a typical 150 mm wafer

Specs	**Value**
Diameter	150 ± 0.5 mm
Thickness	675 ± 25 μm
Orientation	100 ± 1°
Bow	60 μm
Δt	50 μm
Primary flat	55-60 mm
Secondary flat	35-40 mm

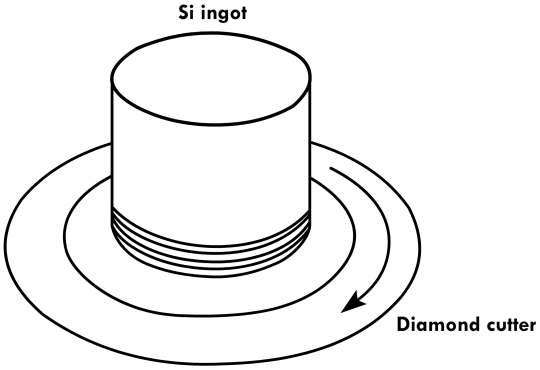

Figure 8: Inner diameter wafer slicing, used for cutting the ingots into individual wafers. The thickness is slightly higher than the final required thickness to account for material loss due to polishing. Adapted from *Microchip fabrication - Peter van Zant.*

contaminated regions. This is usually done in an acid bath with a mixture of hydrofluoric acid, nitric acid, and acetic acid. After etching, the surfaces are polished, first a rough abrasive polish, followed by a chemical mechanical polishing (CMP) procedure. In CMP, a slurry of fine SiO_2 particles suspended in aqueous NaOH solution is used. The pad is usually a polyester material. Polishing happens both due to mechanical abrasion and also reaction of the silicon with the NaOH solution.
Wafers are typically *single side or double side polished.* Large wafers are usually double side polished so that the backside of the wafers can be used for patterning. But wafer handling for double side polished wafers should be carefully controlled to avoid scratches on the backside. Typical 300 mm wafers used for IC manufacture are handled by robot arms and these are made of ceramics to minimize scratches. Smaller wafers (3" and 4" wafers) used in labs are usually single side polished. After polishing, the wafers are subjected to a final inspection before they are packed and shipped to the fab.