Lecture 11: pn junctions under bias

Contents

1 Introduction

A pn junction at equilibrium is characterized by a depletion region where there are no charge carriers (except for those created and annihilated dynamically) and a contact potential. The contact potential is related to the dopant concentration in the p and n sides with higher concentrations leading to larger contact potentials. This, in turn, is related to the position of the Fermi levels in the p and n sides since a higher dopant concentration pushes the Fermi level closer to the valence or conduction band. The pn junction can be biased by connecting to an external circuit and there are two types of biasing (similar to the arguments for the metal-semiconductor Schottky junction)

1. Forward bias
2. Reverse bias

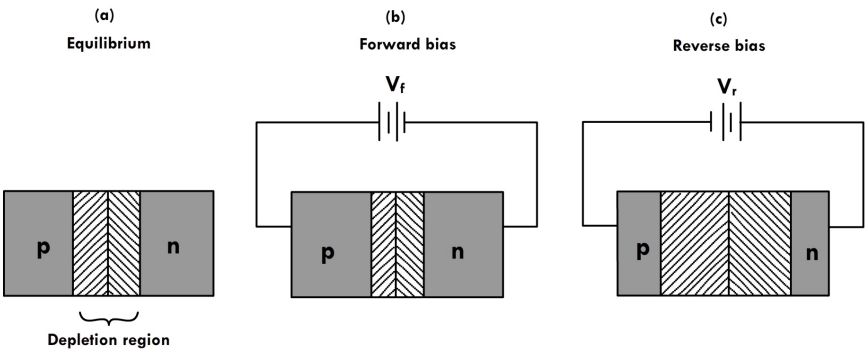

Figure 1: *pn* junction under (a) equilibrium, (b) forward and (c) reverse bias. The depletion width shrinks in forward bias and expands in reverse bias. Adapted from *Semiconductor device physics and design - Umesh Mishra and Jasprit Singh.*

2 Forward bias

Consider a *pn* junction under forward bias. This is achieved by connecting the p side to the positive terminal of an external power source and the n side to the negative terminal. In reverse bias, the connections are interchanged. Equilibrium, forward, and reverse bias connections are shown in figure 1. In the forward bias the external potential (V) *opposes* the contact potential, V_0, that develops in equilibrium. The effect of this is that the net potential at the junction is lowered. In the presence of an external potential the Fermi levels no longer line up but are shifted. This shift can be seen in the band diagram, summarized in figure 2. The application of the external potential, in forward bias, shifts the n side *up* with respect to the p side, see figure 2. This leads to a lowering of the barrier for injection of electrons from the n to the p side (there is a similar lowering of the barrier for holes to be injected from p to n side) and leads to a current in the circuit. This current is due to the **injection of minority carriers** in the *pn* junction.

2.1 Carrier injection

Consider a forward biased *pn* junction showing the change in concentration of carriers along the length of the junction, moving from the p to the n side, figure 3. In equilibrium, the carrier concentrations in the p and n sides are

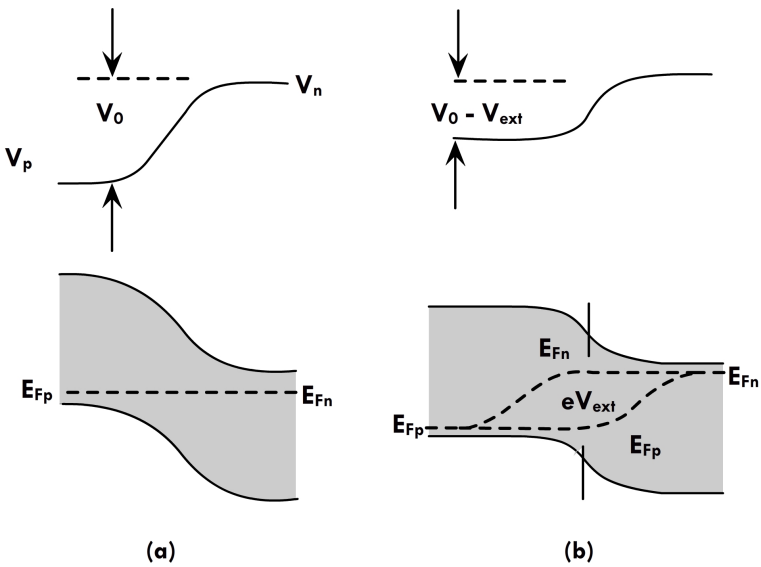

Figure 2: Band diagram of *pn* junction under (a) equilibrium and (b) forward bias. While Fermi levels line up in equilibrium in the presence of an external potential the levels shift by an amount proportional to the applied potential. Adapted from *Semiconductor device physics and design - Umesh Mishra and Jasprit Singh.*

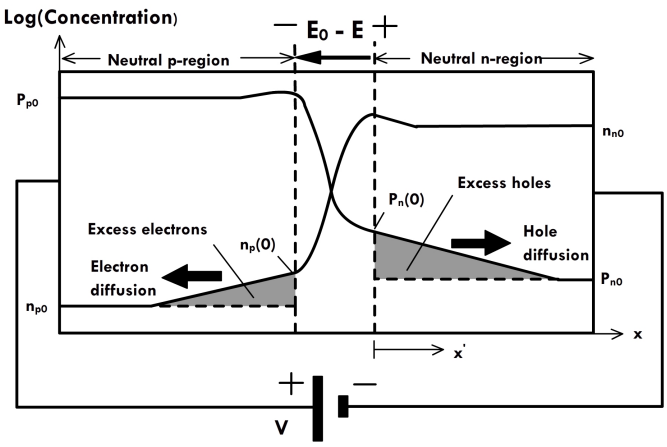

Figure 3: Current in a *pn* junction is due to injection of minority carriers in forward bias. These excess carriers can diffuse before recombining with the majority carriers. Adapted from *Principles of Electronic Materials - S.O. Kasap.*

given by

$$\boxed{\begin{aligned} p_{p0} &= N_A \; ; \; n_{p0} = \frac{n_i^2}{N_A} \\ n_{n0} &= N_D \; ; \; p_{n0} = \frac{n_i^2}{N_D} \end{aligned}} \tag{1}$$

Now, extra carriers are injected due to the forward bias, as shown in figure 3. These extra carriers are minority carriers and diffuse some distance before recombining. These minority carriers constitute the current in a forward biased pn junction since they are constantly being supplied by the external potential . In figure 3, $p_n(0)$ and $n_p(0)$ represent the carriers that are injected due to the applied forward bias. Their concentration is related to the reduced barrier for carrier injection

$$\begin{aligned} p_n(0) &= p_{p0} \; \exp(-\frac{e(V_0 - V_{ext})}{k_B T}) \\ n_p(0) &= n_{n0} \; \exp(-\frac{e(V_0 - V_{ext})}{k_B T}) \end{aligned} \tag{2}$$

where V_0 is the barrier potential and V_{ext} is the external potential during forward bias and the equilibrium concentrations are defined in equation 1. These are minority carriers and diffuse a short distance before getting annihilated. This can be seen in the concentration plot in figure 3 where the initial high concentration at the depletion region interface, $p_n(0)$ and $n_p(0)$, gets reduced to the equilibrium concentration, as we move deeper into the bulk of the n and p regions respectively.
The distance traveled by the minority carriers before recombination is called the **minority carrier diffusion length** (L_h or L_e). Using the usual formulation for one dimensional diffusion this can be written in terms of a diffusion coefficient (D_h or D_e) and carrier lifetime (τ_h or τ_e).

$$\boxed{L_h = \sqrt{D_h \, \tau_h} \; ; \; L_e = \sqrt{D_e \, \tau_e}} \tag{3}$$

The diffusion coefficient is related to the electron and hole mobility values (μ_h and μ_e) by the **Einstein relation**.

$$\boxed{D_h = \frac{k_B T \mu_h}{e} \; ; \; D_e = \frac{k_B T \mu_e}{e}} \tag{4}$$

Consider some typical values for Si. We can the take electron and hole mobilities for undoped Si, where μ_e is 1350 $cm^2 V^{-1} s^{-1}$ and μ_h is 450 $cm^2 V^{-1} s^{-1}$. Using equation 4 the electron and hole diffusivities are calculated to be 34.93

cm^2s^{-1} and 11.64 cm^2s^{-1} respectively. Typical values for the carrier lifetimes (time before the electron or hole recombines and gets annihilated) are of the order of ns. This is different from the carrier scattering time which is of the order of ps (10^{-12} s) and is defined as the time between two successive collisions. A carrier can undergo multiple collisions before recombining. Taking a carrier recombination time of 1 ns the diffusion lengths can be calculated using equation 3. This gives an electron diffusion length of 1.9 μm and hole diffusion length of 1.08 μm. Thus, typical diffusion lengths in a pn junction, where the injected minority carriers recombine, is of the order of μm.

3 Forward bias current

Consider the pn junction schematic shown in figure 3. The excess electron concentration at the interface between the depletion width and the p side is $n_p(0)$ and similarly the excess hole concentration on the n side is $p_n(0)$. These values are given by equation 2. These excess carriers are replenished by the applied voltage of the external circuit so that a current flows through the entire circuit.
Consider the n side of the junction, where the excess minority carriers are holes. When the length of the n region is longer than the diffusion length, the hole concentration at a distance x from the depletion region, marked in figure 3, is given by

$$\begin{aligned} p_n(x) &= p_n(0)\ \exp(-\frac{x}{L_h}) \\ \text{excess holes} \Rightarrow \Delta p_n(x) &= p_n(x) - p_{n0} = \Delta p_n(0)\ \exp(-\frac{x}{L_h}) \end{aligned} \tag{5}$$

The excess holes is above the base hole concentration in the n side, which is very small. The hole diffusion current ($J_{D,\,hole}$) is then defined by the diffusion coefficient and concentration gradient

$$J_{D,\,hole} = -eD_h\frac{dp_n(x)}{dx} = -eD_h\frac{d\Delta p_n(x)}{dx} \tag{6}$$

This is similar to *Fick's first law of diffusion.* Substituting for $p_n(x)$ using equation 5 and evaluating, the hole current is given by

$$J_{D,\,hole} = \frac{eD_h}{L_h}\ \Delta p_n(0)\ \exp(-\frac{x}{L_h}) \tag{7}$$

Similarly, there will be a current due to electron diffusion in the p region, which can be written similar to equation 7. The total diffusion current, which

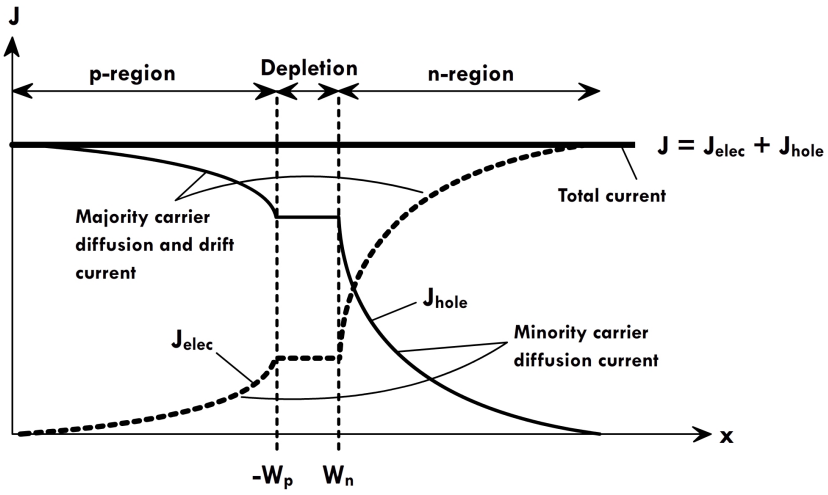

Figure 4: Total diffusion current in a *pn* junction. This is the sum of the electron and hole current and also a drift component due to the electric field. The diffusion current is due to the injection of minority carriers. Adapted from *Principles of Electronic Materials - S.O. Kasap.*

is the sum of the electron and hole current, is a constant and independent of position. This is shown schematically in figure 4.

Thus, the total diffusion current, due to electron and holes, can be evaluated at $x = 0$. The hole diffusion current at this position can be written using equations 7 and 2 and the law of mass action.

$$\begin{aligned} J_{D,\,hole} &= \frac{eD_h}{L_h}\,\Delta p_n(0) = \frac{eD_h}{L_h}\,(p_n(0) - p_{n0}) \\ J_{D,\,hole} &= \frac{eD_h p_{n0}}{L_h}\,[\exp(\frac{eV}{k_BT}) - 1] \\ J_{D,\,hole} &= \frac{eD_h n_i^2}{L_h N_D}\,[\exp(\frac{eV}{k_BT}) - 1] \end{aligned} \tag{8}$$

It is possible to write a similar expression for the current due to the diffusion of electrons. This can be written as

$$J_{D,\,electron} = \frac{eD_e n_i^2}{L_h N_A}\,[\exp(\frac{eV}{k_BT}) - 1] \tag{9}$$

Thus, the total diffusion current, due to both electrons and holes is given by the sum of equations 8 and 9.

$$\boxed{J_D = (\frac{D_h}{L_h N_D} + \frac{D_e}{L_h N_A}) e n_i^2\,[\exp(\frac{eV}{k_BT}) - 1]} \tag{10}$$

This is called the **Schockley equation** and gives the total current due to diffusion in the forward bias and its dependence on the applied voltage. The first part of equation 10 is called the *reverse saturation current density*(J_{s0}).

$$\boxed{\begin{aligned} J_{s0} &= e\, n_i^2 (\frac{D_h}{L_h N_D} + \frac{D_e}{L_h N_A}) \\ J_D &= J_{s0}\, [\exp(\frac{eV}{k_B T}) - 1] \end{aligned}} \tag{11}$$

This forward bias current is due to the diffusion of the minority carriers in the *pn* junction. L_h and L_e are the diffusion lengths of the minority carriers and they are typically smaller than the dimensions of the p and n regions. This is called a *long diode*. If the diode dimensions are smaller than the diffusion lengths, it is called a *short diode*, and L_h and L_e are replaced by l_e and l_h, the diode dimensions.
Some of the minority carriers diffusing across the junction will recombine in the depletion region. These are also replenished by the electrons and holes supplied by the external circuit. This current is called the *recombination current* and is also exponentially dependent on the applied voltage. Combining both terms (diffusion and recombination current) the total current in a forward biased *pn* junction is given by

$$J = J_0 \exp(\frac{eV}{\eta k_B T}) \tag{12}$$

where J_0 is a new constant and η is called an *ideality factor*, with a value *between 1 and 2*. When η is close to 1 the current is mostly diffusion current and when η is close to 2 the current is mostly due to minority recombination. The effect of recombination is to lower the overall current in the *pn* junction. The I-V characteristics in forward bias for different semiconductors is shown as a semilog plot in figure 5. Since the current depends exponentially on the applied voltage, the semilog plot is a straight line with different slopes depending on the semiconductor and value of η.

3.1 Band gap dependence

Consider the reverse saturation current (J_{s0}) shown in equation 11. This contains the term n_i^2, which is the intrinsic carrier concentration. This is a material property, for a given temperature, and depends on the band gap.

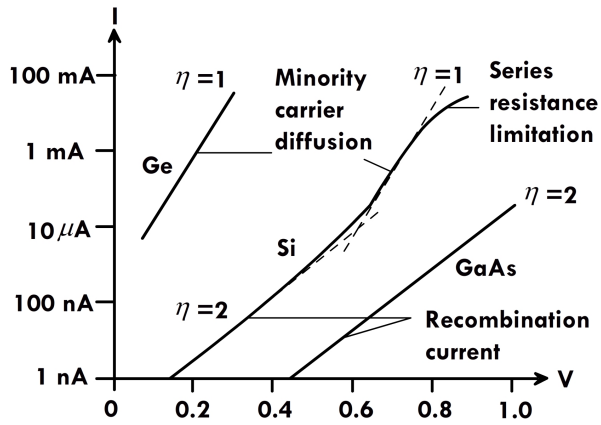

Figure 5: Forward bias I-V plot for a *pn* junction. Adapted from *Principles of Electronic Materials - S.O. Kasap.*

This can be incorporated in the expression for J_{s0}.

$$
\begin{aligned}
J_D &= J_{s0}\,[\exp(\frac{eV}{k_BT}) - 1] \approx J_{s0}\,\exp(\frac{eV}{k_BT}) \\
J_{s0} &= e\,n_i^2(\frac{D_h}{L_hN_D} + \frac{D_e}{L_hN_A}) \\
n_i^2 &= N_c\,N_v\,\exp(-\frac{eV_g}{k_BT}) \\
J_D &= (\frac{D_h}{L_hN_D} + \frac{D_e}{L_hN_A})\,e\,(N_cN_v)\,\exp[\frac{e(V - V_g)}{k_BT}] \\
J_D &= J_1\,\exp[\frac{e(V - V_g)}{k_BT}]
\end{aligned}
\tag{13}
$$

V_g here represents the band gap E_g converted into a potential (dividing by e). The diffusion current then depends on a temperature dependent constant multiplied by a term that depends on the band gap. The forward bias I-V characteristics for different semiconductors are plotted in figure 6. For a given current value, the voltage required is higher with higher V_g (higher band gap).

4 Reverse bias

In forward bias the current increases exponentially with the applied voltage. The external potential opposes the in-built potential and has the effect of

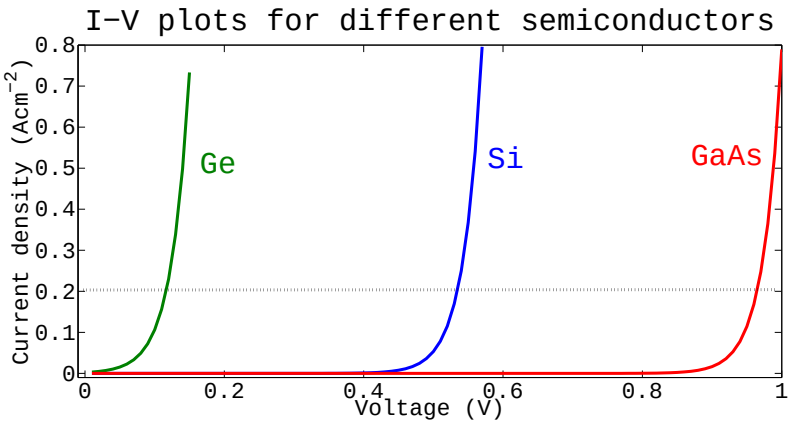

Figure 6: Forward bias I-V plots for *pn* junctions of three different semiconductors. The plots were generated in MATLAB for the same value of donor and acceptor concentrations. The band gap of Ge is 0.66 eV, Si is 1.1 eV and GaAS is 1.43 eV. For a certain current density, shown by dotted lines, the applied voltage required increases with increasing band gap.

lowering the barrier for the electrons and holes. In reverse bias, the applied external potential is in the same direction as the contact potential. This is shown schematically in figure 7. The p side is connected to the negative potential and the n side is connected to the positive potential. The effect of the reverse bias on depletion width is shown schematically in figure 1. The reverse bias causes the depletion region width to increase since the majority carriers are attracted to the external potential. In the energy band diagram the Fermi levels are shifted, as shown in figure 8. This is opposite to the direction of forward bias, shown in figure 2. Because of the higher barrier, diffusion current is negligible in reverse bias. There is however a small current that flows through the *pn* junction, called the **reverse saturation current**. This current is a constant (independent of reverse bias voltage) and is generated by **drift** of the thermally generated carriers in the depletion region. Electron and holes dynamically generated in the depletion region get accelerated towards the n and p side due to the applied voltage and this leads to a small reverse saturation current, also called **drift current**. This is given by J_{s0}, shown in equation 11.

$$\boxed{J_{s0} \;=\; e\, n_i^2 \left(\frac{D_h}{L_h N_D} \;+\; \frac{D_e}{L_h N_A}\right)} \tag{14}$$

This is typically orders of magnitude smaller than the forward bias current. The I-V characteristics of a *pn* junction, for both forward and reverse bias, is

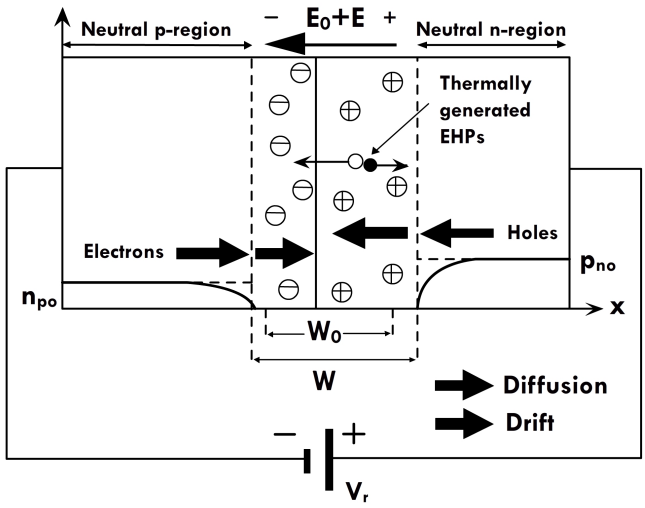

Figure 7: Reverse bias configuration for a *pn* junction. The total potential at the depletion region is increases. This has the effect of increasing the depletion width making it harder for carriers to cross the junction. Adapted from *Principles of Electronic Materials - S.O. Kasap.*

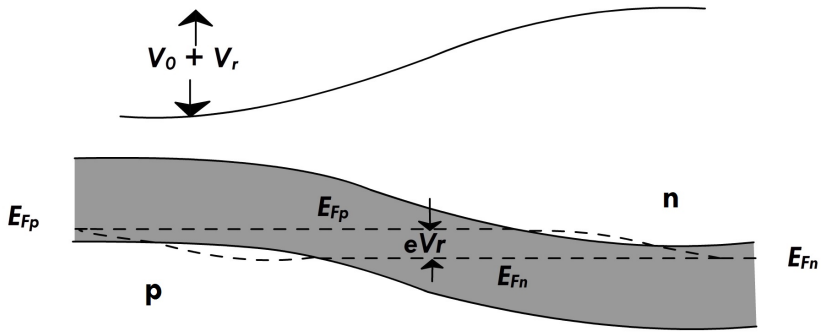

Figure 8: Band diagram of *pn* junction under reverse bias. The Fermi level on the *n* side shifts down leading to a overall increase in the junction potential. Adapted from *Semiconductor device physics and design - Umesh Mishra and Jasprit Singh.*

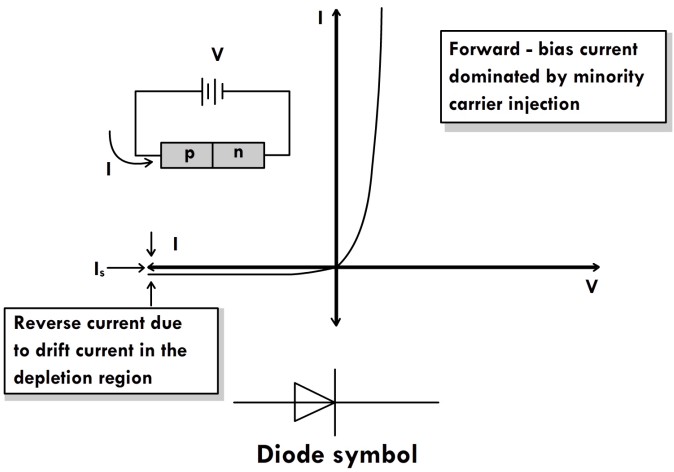

Figure 9: I-V characteristics of a *pn* junction. The diode symbol is shown in the inset. There is an exponentially increasing current in forward bias while the reverse bias current is orders of magnitude smaller. Adapted from *Semiconductor device physics and design - Umesh Mishra and Jasprit Singh.*

shown schematically in figure 9. The forward bias current is orders of magnitude higher than the reverse bias current so that a *pn* junction acts as a **rectifier**. It conducts only in one direction (forward) and does not conduct in the other direction (reverse). The energy band information is summarized in figure 10.

Consider an example of Si *pn* junction, operating at room temperature. The acceptor concentration is 10^{16} cm^{-3} and the donor concentration is 10^{15} cm^{-3}, on the p and n side respectively. While the carrier mobility normally decreases with doping, we can use the mobility values for intrinsic Si, i.e. $\mu_e = 1350\ cm^2V^{-1}s^{-1}$ and $\mu_h = 450\ cm^2V^{-1}s^{-1}$. The minority carrier lifetime is typically of the order of ns, we can use $\tau_e = 50\ ns$ and $\tau_h = 100\ ns$. Since this is Si at room temperature, $n_i = 10^{10}\ cm^{-3}$, the intrinsic carrier concentration. Using equations 3 and 4 it is possible to calculate the carrier diffusion lengths and diffusivites. Substituting these values in equation 11, it is possible to calculate the reverse saturation current density to be $2.15 \times 10^{-10}\ Acm^{-2}$. This is a very small current that is present in reverse bias. The forward bias current increases exponentially with applied voltage. The exponential dependence can be clearly seen in a semilog plot and it is plotted along with the overall I-V behavior in figure 11.

Both the *pn* and Schottky junction show rectification behavior on appli-

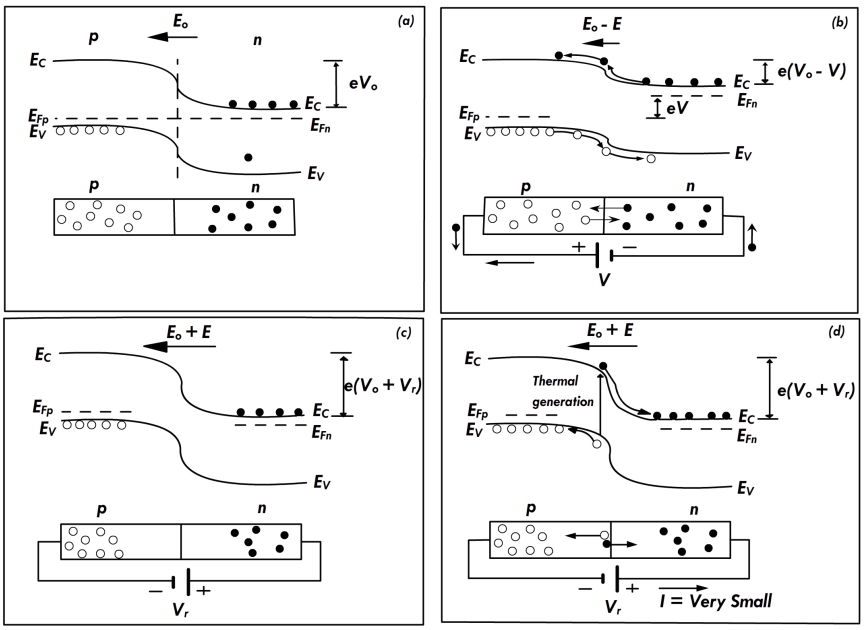

Figure 10: Energy band diagram of a *pn* junction under (a) equilibrium, (b) forward bias, and (c) reverse bias. (d) The reverse saturation current due to thermal generation of carriers is shown. Adapted from *Principles of Electronic Materials - S.O. Kasap.*

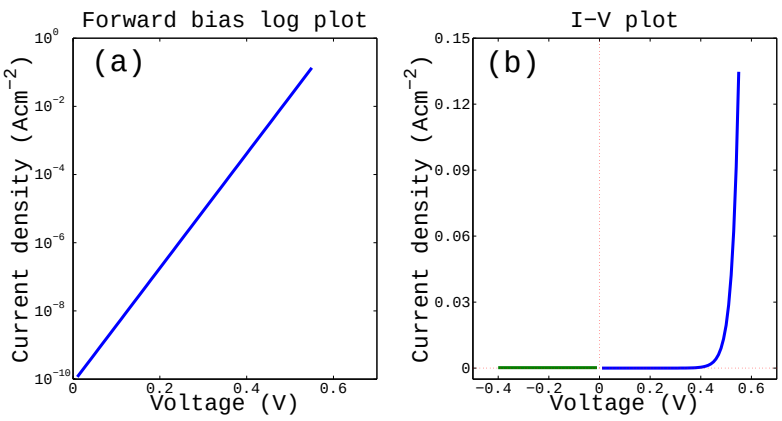

Figure 11: (a) Semilog plot of forward bias current vs. voltage for Si *pn* junction. The exponential increase in current with voltage is seen in the straight line plot. (b) I-V characteristics of the *pn* junction. The forward bias current is orders of magnitude higher than the reverse bias current. The plots were generated in MATLAB.

cation of an external potential. In both cases the behavior arises from the lowering of the potential barrier on application of forward bias and the current increases exponentially with voltage. For these junctions, it is possible to define a **rectification ratio**, which is the ratio of the forward bias to reverse bias current, for the same absolute voltage value. *pn* junctions have a typical rectification ratios of $10^7 - 10^{10}$, while Schottky junctions have values around $10^3 - 10^6$, making *pn* junctions a better rectifier than metal-semiconductor Schottky junctions.