

EFFECT OF ANNEALING AND OF COOLING RATES ON *n*-GaAs ELECTRODE PHOTOELECTROCHEMICAL CHARACTERISTICS

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The effect of annealing of the *n*-GaAs semiconductor on its characteristics in photoelectrochemical (PEC) systems has been investigated. The photocurrent densities vs. potential plots were improved by annealing. Cell efficiency and short-circuit current densities were enhanced for the annealed *n*-GaAs.

The effect of the rate of cooling of heated *n*-GaAs wafers was also investigated. It was found that the slowly cooled electrodes gave better dark current density vs. potential plots, for samples annealed below 600 °C. For samples annealed at higher temperatures, quenching gave better dark-current density vs. potential plots. For *n*-GaAs, slowly cooled electrodes from temperatures below 600 °C showed better photocurrent density vs. potential plots and higher efficiency. *n*-GaAs samples, quenched from temperatures above 700 °C, showed better photocurrent density vs. potential plots and higher efficiency than their slowly cooled counterparts.

Keywords: *n*-GaAs; Annealing; Rate of cooling; Photocurrent; Dark current

1 INTRODUCTION

The rate of cooling of heated metal crystals affects the crystal properties. For example, it is known that quenching (rapid cooling) of heated aluminum bars prevents contraction to original lengths [1, 2]. The metastable spheres in the heated crystal may not return to their original stable positions with quenching. Alternatively, slow cooling allows the return of metastable spheres to their original positions. Therefore, slow cooling is expected to improve the characteristics of metallic conductors.

Annealing of SC wafers was reported to enhance their characteristics, such as crystal structure, surface and doping distribution [3–9]. Slow cooling has also been reported to enhance SC characteristics, *vide infra*.

We hereby wish to utilize such discussions to improve the PEC characteristics of the *n*-GaAs semiconductor. Such a technique has not been widely used as a tool to enhance

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the PEC characteristics of semi-conducting materials [10]. It is assumed that slowly cooled crystals may regain their original order. On the other hand, quenched crystals will retain imperfections. Such imperfections will be exhibited in many ways, such as ill-defined band-edge structures, distorted crystal surfaces and increased surface states. This will consequently affect the dark- and photo-current/potential plots.

2 EXPERIMENTAL

2.1 Materials and Electrode Preparation

LiCl_4 , $\text{K}_3\text{Fe}(\text{CN})_6$ and $\text{K}_4\text{Fe}(\text{CN})_6$ were purchased from Aldrich, Al_2Se_3 from Alfa Vantor, and HCl from Frutarom. All organic solvents (methanol, dichloromethane, DMF) were obtained from Riedel–DeHaën in a pure form.

The redox couple solution was prepared as shown in the literature [11, 12]. 1.0 M $\text{KOH}/1.0 \text{ M Se}^{2-}$ solution was prepared by adding $\text{HCl}_{(\text{aq})}$ to $\text{Al}_2\text{Se}_{3(\text{s})}$ to generate $\text{H}_2\text{Se}_{(\text{g})}$ *in situ*, and then bubbled through a 3.0 M KOH solution. The oxidized form of the Se_2^{2-} couple was obtained by exposing $\text{KOH–Se}_{(\text{aq})}^{2-}$ solution to air until the solution acquired a red-brown color.

n-GaAs substrates were mono-crystalline single surface mirror polished Si-doped wafers of *n*-GaAs ($N_d = 3.6 \times 10^{17} \text{ cm}^{-3}$ for the front and $1.8 \times 10^{18} \text{ cm}^{-3}$ for the tail). The mono-crystalline plates, 50 mm round shape were oriented to expose the $\langle 100 \rangle$ face. The mobility was $2.6 \times 10^3 \text{ cm}^2/\text{V s}$ in the front and $2.6 \times 10^3 \text{ cm}^2/\text{V s}$ in the tail. The electrodes were fabricated as follows: the wafers were cut into small pieces ($\sim 0.1 \text{ cm}^2$).

The pieces were then annealed at the desired temperatures. A closed clay crucible was inserted in a long stainless steel cylinder, with an SC wafer to be annealed inside. Annealing was conducted using a thermostated horizontal tube furnace. The heat was raised to the desired temperature (400 °C, 500 °C, 600 °C, 700 °C, or 800 °C), under a clean atmosphere of N_2 and was left at that temperature for 20 min before cooling. The system was left to cool, in the desired method (slow cooling or quenching) under a continuous flow of N_2 .

In slow cooling, the heated samples were cooled in steps of 50 °C, and the annealing system was left for 20-min intervals at each cooling step under nitrogen flow. The time intervals of the slow cooling process were varied from 8–12 h, depending on the annealing temperature.

In fast cooling, the stainless steel cylinder (with clay crucible and semiconductor wafer inside) was quenched by dipping into a water path. The semiconductor wafer was cooled to room temperature within 2 min, from the desired temperature, under a slow flow of N_2 .

After cooling to room temperature, the semiconductor piece was mounted to a copper plate (welded to a copper wire), using Ga–In eutectic on both the copper plate and the semiconductor unpolished (back) surface [13]. The copper wire was Teflon-insulated. The exposed Cu and Ga–In eutectic with semiconductor edges of the electrode were then sealed with epoxy cement to expose only the electrode polished mirror face to the solution. The electrodes were left to dry for at least 24 hours at room temperature under nitrogen. The sealed electrodes were then rinsed with methanol to remove possible solvent containment from the epoxy, and then dried with a slow stream of N_2 .

n-GaAs electrodes were etched prior to use by $\text{Br}_2/\text{CH}_3\text{OH}$ (0.05% v/v) solution [11]. The electrode was immersed in the $\text{Br}_2/\text{CH}_3\text{OH}$ solution for about 5 s, rinsed with distilled water and then dipped into (1.0 M) KOH solution. The above procedure was repeated three times to obtain a shiny mirror surface. The electrode was then rinsed with distilled water and methanol, and dried with nitrogen.

2.2 Equipment

Current–voltage data were measured using a computer-controlled Princeton Applied Research (PAR) 263A potentiostat. A Lutron LX-102 light meter was used to measure the light intensity in lux units. The light meter was calibrated against a Kipp and Zonen CM11 pyranometer. The pyranometer measures radiance in watt m^{-2} [14, 15]. The illuminant used in our experiments was measured in lux and calibrated into irradiant in watt cm^{-2} units.

A three-electrode one-compartment photoelectrochemical cell, (involving a platinum counter electrode, a reference standard calomel (SCE) electrode and an SC working electrode) was used in J – V measurements. $\text{KOH}/\text{Se}^{2-}/\text{Se}_2^{2-}$ was the redox couple for n -GaAs working electrodes.

A 50 W Xenon lamp with housing and a convex lens was used for illumination. The illumination on the electrode was 8500 lux.

The J – V measurements were conducted at room temperature, under nitrogen atmosphere. The dark experiments were performed with complete exclusion of light, by covering the system with a black cloth. On the other hand, a 50 W Xenon lamp was used in the photocurrent measurements.

3 RESULTS

In this study, n -GaAs electrodes have been treated by heating and cooling at different rates. The SC wafers were heated to a desired temperature (400 °C, 500 °C, 600 °C, 700 °C, or 800 °C). Cooling of the heated wafers to room temperature (~ 25 °C) was done using two different methods (quenching and slow cooling).

The effect of treatment on the SC characteristics was measured by monitoring different parameters dark J – V and photo J – V plots.

3.1 Dark J – V Plot Enhancement

3.1.1 Annealing Effect

Preheated n -GaAs samples showed better dark J – V plots than the untreated n -GaAs.

n -GaAs samples, from 700 °C and 800 °C, showed better dark J – V plots compared to untreated samples (Fig. 1). No significant difference can be noticed between the J – V plot of the untreated sample and the J – V plots of samples quenched from temperatures of 600 °C or lower. n -GaAs samples, slowly cooled from any preheating temperature in the range 400–800 °C, have better J – V plots than the untreated samples (Fig. 2).

3.1.2 Effect of Rate of Cooling from 600 °C or Lower

n -GaAs samples, slowly cooled from 600 °C or lower, show better dark J – V plots than their quenched counterparts. Figures 3–5 showed dark J – V plots of slowly cooled and of quenched samples from 400 °C, 500 °C, and 600 °C, respectively.

3.1.3 Effect of Rate of Cooling from 700 °C or Above

Dark J – V plots for n -GaAs samples quenched from 700 °C or higher, are better than their slowly cooled counterparts. Figures 6 and 7 show dark J – V plots for slowly cooled samples and for quenched samples from 700 °C and 800 °C, respectively.

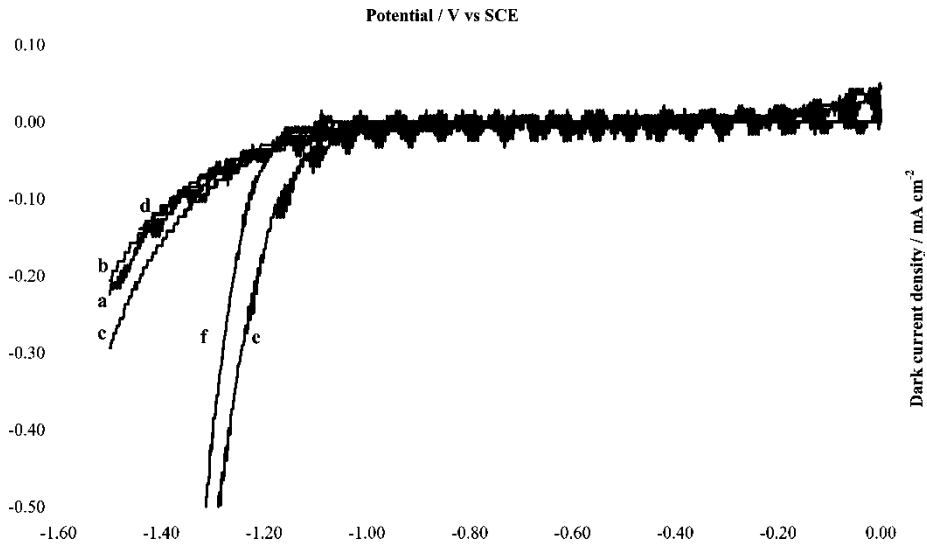


FIGURE 1 Dark J - V plots for a unheated n -GaAs. Quenched n -GaAs samples from b 400 °C, c 500 °C, d 600 °C, e 700 °C, and f 800 °C. All J - V measurements were conducted in $K_2Se/K_2Se_2/KOH$ at 25 °C.

3.2 Photo J - V Plot Enhancement

3.2.1 Annealing Effect

Preheated n -GaAs samples showed better photo J - V plots than untreated samples.

Photo J - V plots (Fig. 8), observed for n -GaAs samples quenched from 700 °C and 800 °C are better than the untreated counterparts. Photo J - V plots, measured for samples quenched from 600 °C or lower, are not significantly different from untreated counterparts. n -GaAs samples, slowly cooled from any preheating temperature, have better photo J - V plots (Fig. 9) than the untreated counterpart.

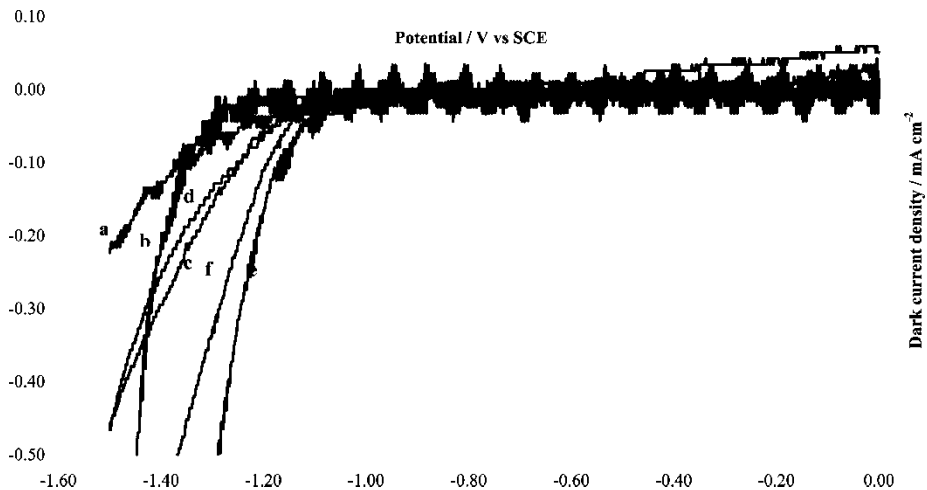


FIGURE 2 Dark J - V plots for a unheated n -GaAs. Slowly cooled n -GaAs samples from b 400 °C, c 500 °C, d 600 °C, e 700 °C, and f 800 °C. All J - V measurements were conducted in $K_2Se/K_2Se_2/KOH$ at 25 °C.

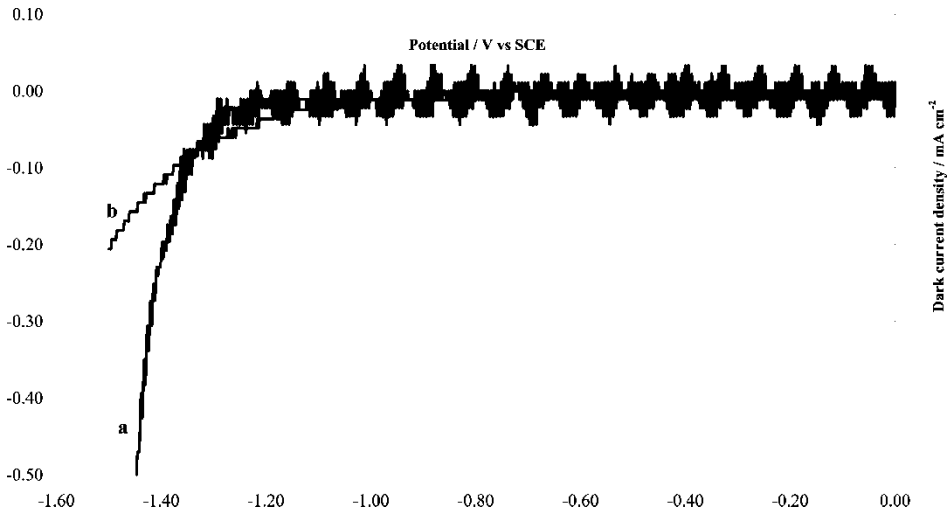


FIGURE 3 Dark J - V plots of a slowly cooled and b quenched n -GaAs from 400 °C. All J - V measurements were conducted in $K_2Se/K_2Se_2/KOH$ at 25 °C.

3.2.2 Effect of Rate of Cooling from 600 °C or Below

n -GaAs samples, slowly cooled from 600 °C or lower, have better photo J - V plots than their quenched counterparts. Figures 10–12 show the photo J - V plots for slowly cooled samples and for quenched samples from 400 °C, 500 °C, and 600 °C, respectively.

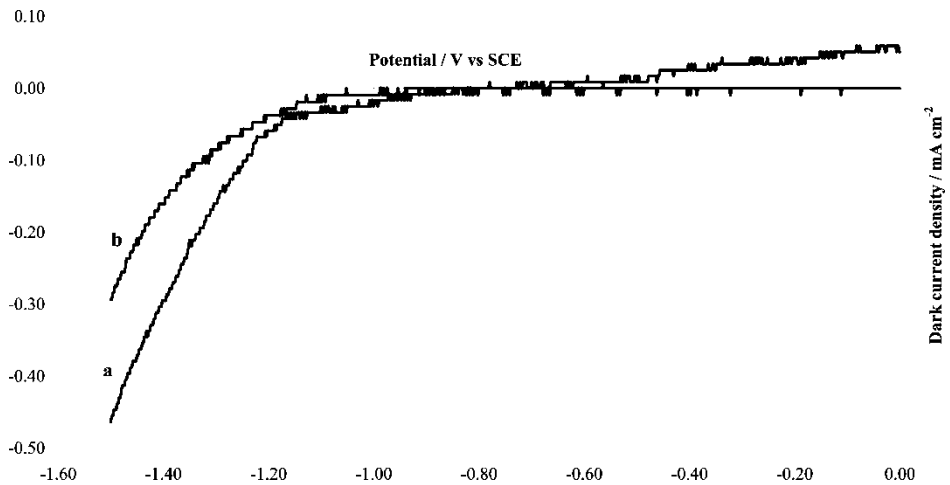


FIGURE 4 Dark J - V plots of a slowly cooled and b quenched n -GaAs from 500 °C. All J - V measurements were conducted in $K_2Se/K_2Se_2/KOH$ at 25 °C.

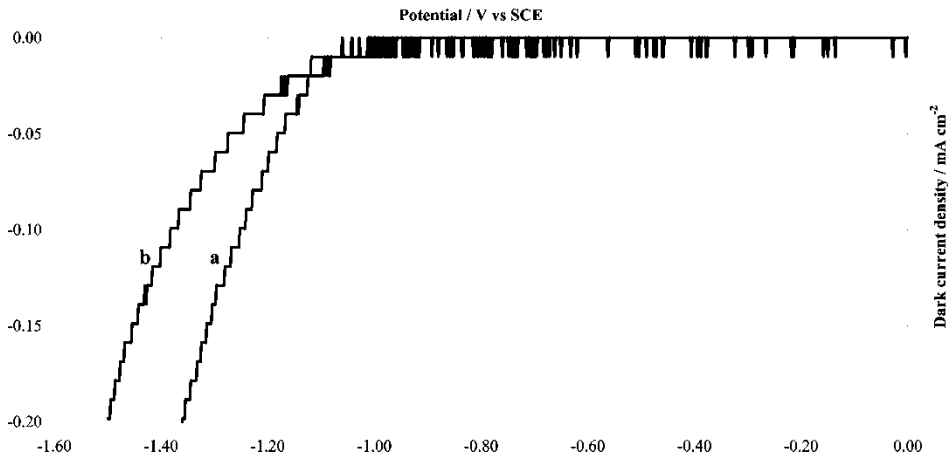


FIGURE 5 Dark $J-V$ plots of **a** slowly cooled and **b** quenched n -GaAs from 600 °C. All $J-V$ measurements were conducted in $K_2Se/K_2Se_2/KOH$ at 25 °C.

3.2.3 Effect of Rate of Cooling from 700 °C or Above

n -GaAs samples, quenched from temperatures higher than 700 °C show better photo $J-V$ plots than their slowly cooled counterparts. This is clearly exhibited in Figures 13 and 14 for preheated samples from temperatures 700 °C or above.

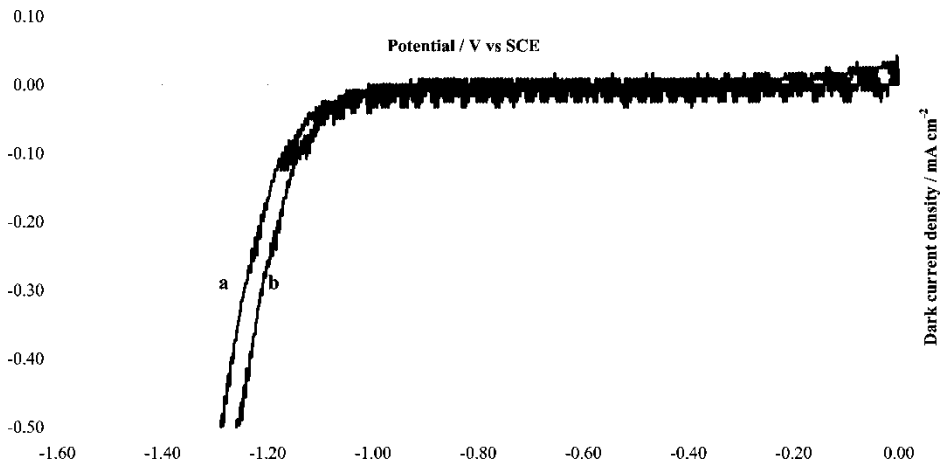


FIGURE 6 Dark $J-V$ plots of **a** slowly cooled and **b** quenched n -GaAs from 700 °C. All $J-V$ measurements were conducted in $K_2Se/K_2Se_2/KOH$ at 25 °C.

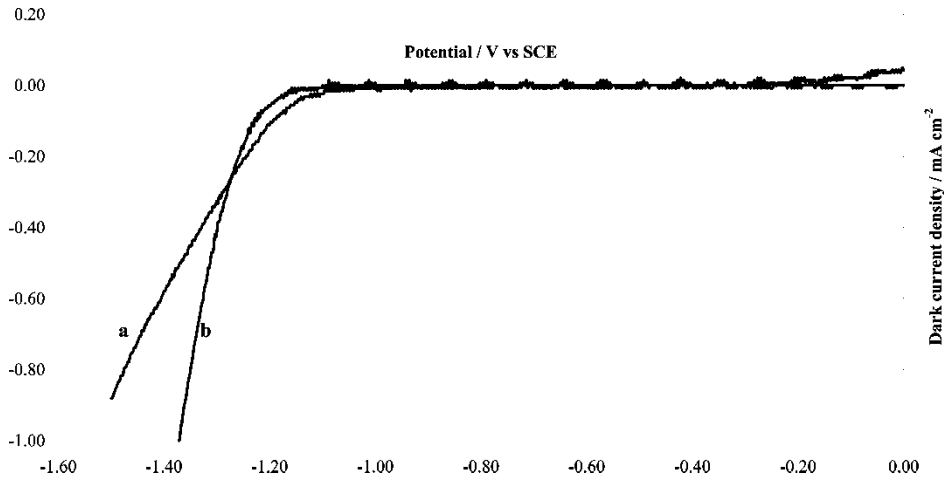


FIGURE 7 Dark J - V plots of a slowly cooled and b quenched n -GaAs from $800\text{ }^{\circ}\text{C}$. All J - V measurements were conducted in $\text{K}_2\text{Se}/\text{K}_2\text{Se}_2/\text{KOH}$ at $25\text{ }^{\circ}\text{C}$.

4 DISCUSSION

4.1 Effect of Annealing on J - V Plots

Annealing of semiconductor wafers enhances the crystal homogeneity, quality, performance and reliability. Annealing also reduces defects, and lowers surface roughness. This has been reported in the literature.

Photo-thermal processing may provide better performance and higher reliability of SC devices [3]. Annealing SC in ultra high vacuum chambers at about $700\text{ }^{\circ}\text{C}$ effectively lowered the SC surface roughness [4]. Annealing [5] reduces the number of Si interstitial atoms inside Si crystals. It is reported that thermal annealing plays an important role in the crystallization process of homogeneous ultra thin a-Si:H sublayers [6]. Das *et al.* [9] found that, for thin

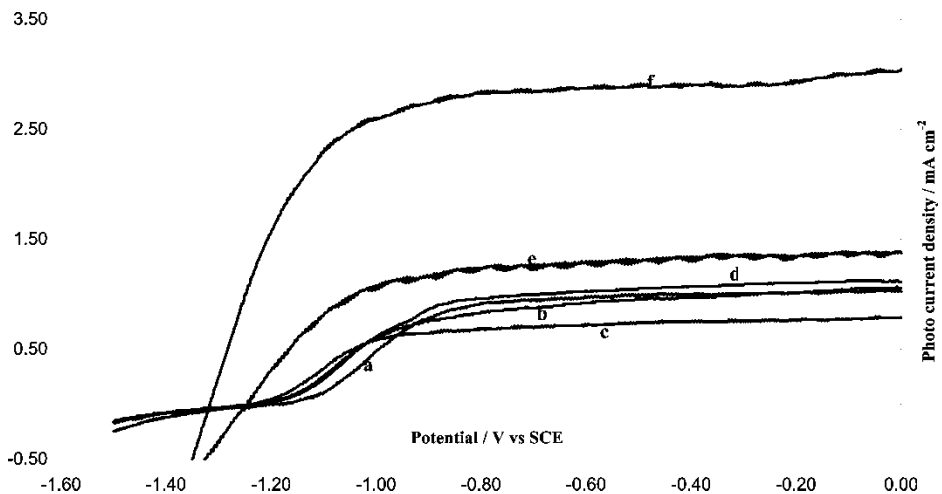


FIGURE 8 Photo J - V plots for a untreated n -GaAs sample. Quenched n -GaAs samples from b $400\text{ }^{\circ}\text{C}$, c $500\text{ }^{\circ}\text{C}$, d $600\text{ }^{\circ}\text{C}$, e $700\text{ }^{\circ}\text{C}$, and f $800\text{ }^{\circ}\text{C}$. All J - V measurements were conducted in $\text{K}_2\text{Se}/\text{K}_2\text{Se}_2/\text{KOH}$ at $25\text{ }^{\circ}\text{C}$.

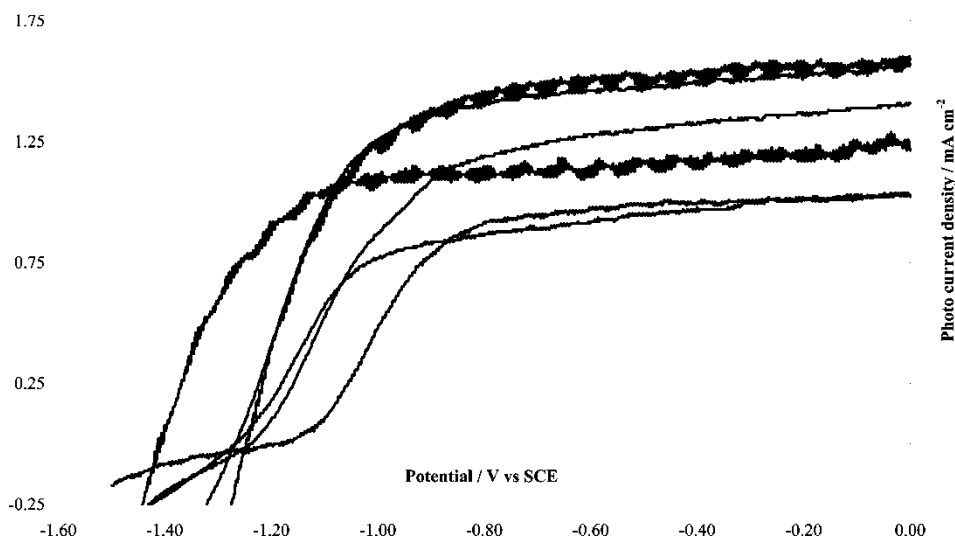


FIGURE 9 Photo J - V plots for **a** untreated n -GaAs sample. Slowly cooled n -GaAs samples from **b** 400 °C, **c** 500 °C, **d** 600 °C, **e** 700 °C, and **f** 800 °C. All J - V measurements were conducted in $K_2Se/K_2Se_2/KOH$ at 25 °C.

films of n -InSe, surface treatment such as etching and annealing leads to increased efficiency of the PEC solar cell, at a pH value of 6.2. Quality, optical properties and structures of different SC crystals have been improved by annealing [7, 8]. The results obtained in this report were consistent with these reports.

Annealing n -GaAs samples improved the characteristics of the electrode. This was observed despite the method of cooling of the annealed samples. For quenched samples, the effect is more pronounced, especially for higher heating temperatures. Figure 1 indicates that the dark J - V plots were improved by annealing at higher temperatures (700–800 °C). In the case of slow cooling, it was found that the annealed n -GaAs samples (at temperatures

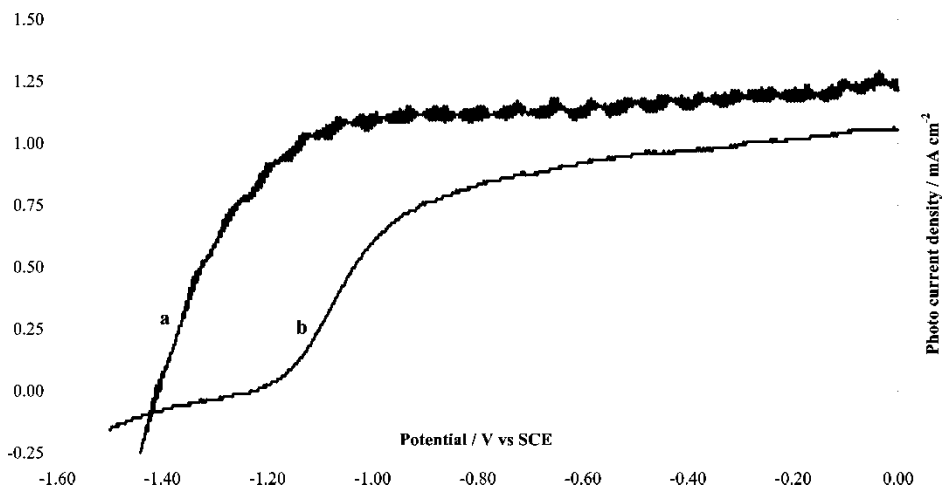


FIGURE 10 Photo J - V plots of **a** slowly cooled and **b** quenched n -GaAs from 400 °C. All J - V measurements were conducted in $K_2Se/K_2Se_2/KOH$ at 25 °C.

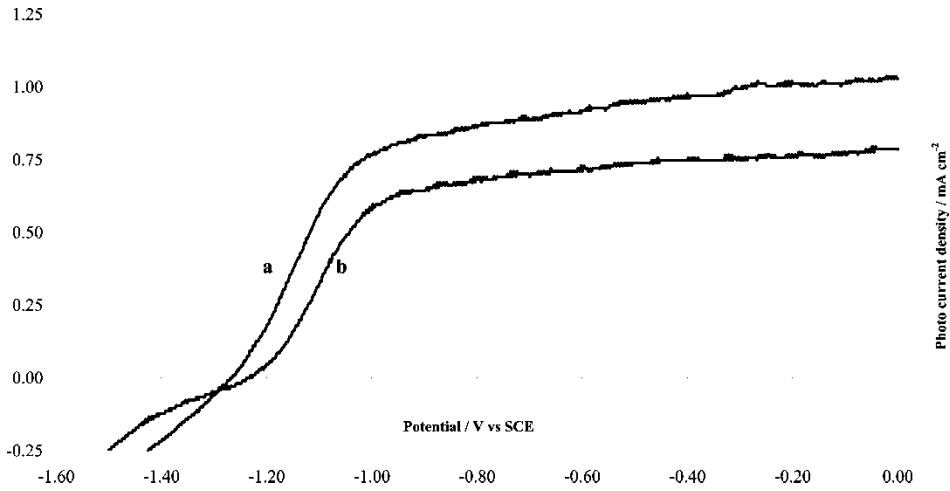


FIGURE 11 Photo J - V plots of **a** slowly cooled and **b** quenched n -GaAs from 500°C . All J - V measurements were conducted in $\text{K}_2\text{Se}/\text{K}_2\text{Se}_2/\text{KOH}$ at 25°C .

in the range 400 – 800°C) give better dark J - V plots than their untreated counterparts. Figure 2 indicates that the dark J - V plots were improved for all the used annealing temperatures. Generally, annealing of n -GaAs samples improves their dark J - V plots. As annealing temperature increases, the dark J - V plots become better. Such enhancement in dark J - V plots is presumably due to enhancement of crystal structure by annealing. Annealing of n -GaAs reduces crystal defects, dislocation density and surface roughness as reported by literature [3–9]. This in turn improves dark currents.

Similar behavior was observed in photo J - V plots, as shown in Figures 8 and 9. Annealing n -GaAs wafers improved the photo J - V plots. Values of short-circuit photo-current density were enhanced by annealing the SC. As discussed above, annealing the SC improves the crystal by lowering defects and reducing surface states. This will in turn lower the electron-hole recombination and enhance charge separation.

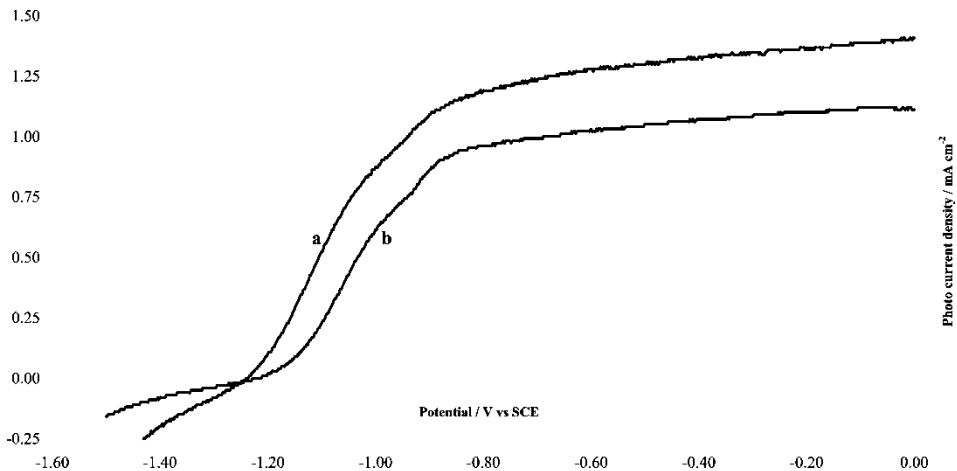


FIGURE 12 Photo J - V plots of **a** slowly cooled and **b** quenched n -GaAs from 600°C . All J - V measurements were conducted in $\text{K}_2\text{Se}/\text{K}_2\text{Se}_2/\text{KOH}$ at 25°C .

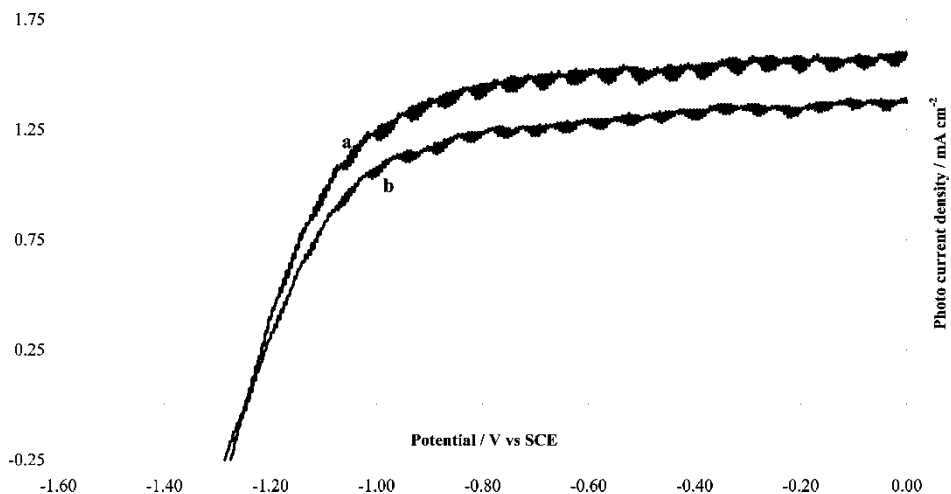


FIGURE 13 Photo J - V plots of **a** slowly cooled and **b** quenched n -GaAs from 700°C . All J - V measurements were conducted in $\text{K}_2\text{Se}/\text{K}_2\text{Se}_2/\text{KOH}$ at 25°C .

4.2 Effect of Cooling Rate

Many SC crystal parameters are affected by cooling rates. Examples of such parameters are: composition uniformity, growth film thickness, and luminescence properties. The dislocation density and concentration of structural defects also depend on the cooling rate of SC crystals.

Literature indicates that slow cooling improves SC crystallinity and lowers dislocation density of semiconductor crystals. Kita *et al.* [16] showed that a uniform film growth of Si from Cu-Si solution, with constant temperature gradient distribution, at the cooling rate of $0.1^{\circ}\text{C}/\text{s}$ and $0.05^{\circ}\text{C}/\text{s}$ (low cooling rate), was possible. It is possible to obtain an InGaAs crystal with a uniform composition in the growth direction by adjusting the cooling rate of the growth zone to be $0.2^{\circ}\text{C}/\text{h}$ (low cooling rate) [17]. Slow cooling of InP/Si heteroepitaxial crystals, from 650°C , reduces the dislocation density [18]. Slow cooling of SiGe, grown using liquid phase epitaxy onto Si, gave lower threading dislocation

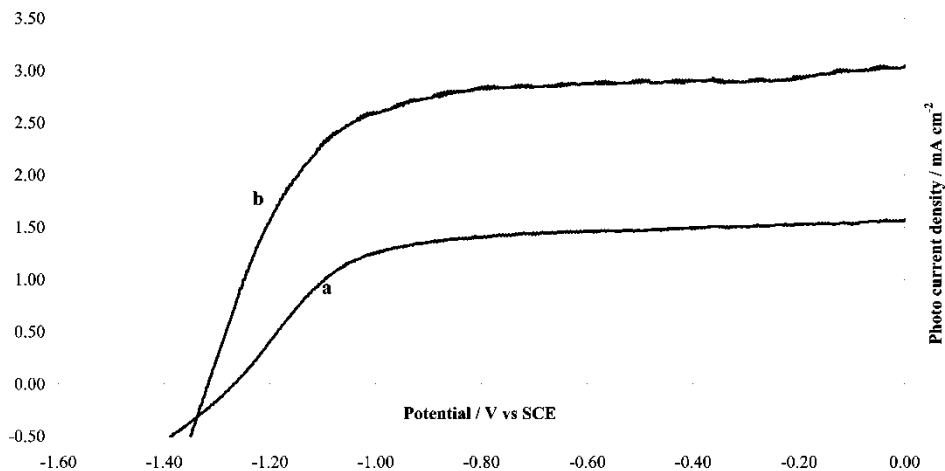


FIGURE 14 Photo J - V plots of **a** slowly cooled and **b** quenched n -GaAs from 800°C . All J - V measurements were conducted in $\text{K}_2\text{Se}/\text{K}_2\text{Se}_2/\text{KOH}$ at 25°C .

densities [19]. With slower cooling rates, the dislocation-assisted photoluminescence intensity was lowered, whereas the transverse optical phonon and the no-phonon photoluminescence intensity was higher [19]. With higher cooling rates, higher surface phase shifts were observed in Si samples [20]. Lee *et al.* [21] showed that the dark current could be greatly reduced through rapid thermal annealing of porous silicon. The results observed in this work are consistent with these literature reports to some extent, *vide infra*.

4.2.1 Cooling from 600 °C or Below

Slowly cooled n-GaAs samples, from temperature 600 °C or below, showed better dark J - V plots than their quenched counterparts, as shown in Figures 3–5. This is consistent with literature [16–21].

Slow cooling of the n-GaAs samples allows enough time for metastable atoms of annealed samples to return to equilibrium positions at the storage temperature [1]. This in turn will minimize structural defects, and dislocations created during growth and annealing. On the other hand, quenched samples will keep the atoms in their new positions after annealing. Quenching will deprive the metastable atoms from any pathways to return to their stable positions. The defect density in quenched samples will therefore be greater than their slowly cooled counterparts. Thus, slow cooling reduces the surface state density. Such an effect will improve n-GaAs crystallinity, and therefore enhances dark current density.

Photo J - V plot results (Figures 10–12) show that the slowly cooled n-GaAs samples, from temperature 600 °C or below, exhibited better photo J - V plots with higher efficiency than their quenched counterparts. These results support the discussions and results presented for dark J - V plot enhancement shown earlier. Slower cooling yields better crystal structures with lower surface state densities and higher short-circuit current densities.

4.2.2 Cooling from 700 °C or Above

Quenched n-GaAs samples, from temperatures above 650 °C, had better dark J - V plots than their slowly cooled counterparts. Figures 6 and 7 indicate these results. Slow cooling of annealed n-GaAs samples allows longer exposure to higher temperatures, and consequently, diffusion of impurities may increase. Vacancy and interstitial diffusion represent such diffusion, in addition to diffusion of n-GaAs atoms themselves. This in turn causes the formation of dislocations in addition to point defects in slowly cooled samples. Thus exposure of n-GaAs to annealing temperatures 700 °C or above, for longer times, will increase dislocation and point defect densities. Presence of high density of dislocation will affect the sample crystallinity. Consequently, the surface state density will increase at the SC/liquid interface, and will lower the quality of dark J - V plots. On the other hand, quenching of annealed samples from temperatures 700 °C or above will minimize diffusion. Thus fewer dislocations or point defects will be formed. So quenching of n-GaAs samples from temperatures 700 °C or above improves the n-GaAs crystallinity, and consequently improves dark J - V plots.

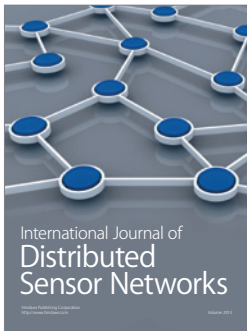
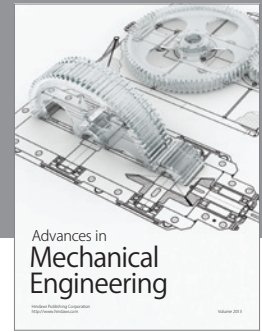
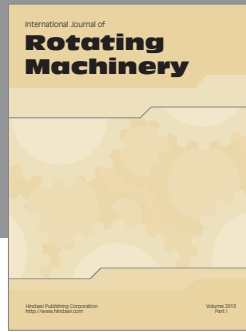
These explanations have direct evidence from photo J - V plot results. Figure 13 shows that quenched n-GaAs samples from 700 °C exhibited almost the same photo J - V plot as the slowly cooled counterpart. Figure 14 shows that the quenched n-GaAs sample from 800 °C exhibited a better photo J - V plot with higher efficiency than the slowly cooled counterpart. Better photo J - V plots and higher efficiencies are indications of lower surface state densities at the SC/liquid interface, and consequently, lower dislocations and lower point-defect densities.

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