Special topics (26483)
Microelectronic fabrication

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Outlines:

Expected Course outcome (Objectives): The student expected to have a clear overview of the microelectronic fabrication process. Also the student will be able to Understand the physics of each key step in the process. In addition, the student will be able to understand new technologies by self-learning in the future.

Primary text:

Other references:
"Microelectronic Processing", W.S. Ruska, McGraw-Hill

Prerequisite:
Students need understanding of basic transistor & diode operation.
Intended topics to be covered:

1: Clean Room Technology & Silicon Wafer Production
- Basic outline of fabrication process: with to real structures.
- Theory behind clean room operations:
- History of semiconductor devices: diodes, transistors, Germanium/Silicon transition, monolithic integrated circuits
- Basic operation of Transistors, diodes
- Projected trends in Fabrication
- Theory and operations for contamination elimination, and safety issues.
- Silicon wafers; Crystallography, Production and Defects:
- Basic silicon wafer parameters, solid solubility of dopants in silicon, defects, and basic economics of operations.

2: Thermal Oxidation
- Basic theory of the silicon oxidation, practical operations and measurement of films (thickness and quality).

3: Lithography
- Basic operation of photolithography, chemical basis of photoresist, exposure equipment, exposure/development theory, and problems
4: Advanced Lithography
• Dealing with defects and exposure effects
• Advanced Lithography, Deep UV, Extreme UV, X-ray

5: Etching
• Theory and operations of etching in general;
• Wet (chemical) etching of oxides

6: Etching II
• Wet etching of silicon and metals

7: Diffusion Processes & Ion Implantation
• Diffusion theory (constant, limited source, multisource).
• Theory and operation of Ion implantation doping techniques.

8: Thin Film Deposition: Evaporation and Sputtering
• Theoretical and experimental operation of vacuum systems.
• Theory and operation of evaporation and sputtering systems

9: Thin Film Deposition: Chemical Vapor Deposition
• Theory and operation of Chemical Vapor Deposition (CVD), Plasma Enhanced CVD
• Film thickness measurement and film problems
10: Epitaxy CVD and Dry Etching Processes
• Epitaxy (deposition with same crystal structure) & laser CVD
• Dry etching processes (Plasma, Sputtering and Reactive Ion)

11: Packaging, Yields, Processing Silicon Foundries
• Testing, dicing of wafers, packaging, bonding, yield theory and measurements.
• Silicon Foundries

12: CMOS and Bipolar Process Integration in practice
• Layer by layer process of sample CMOS and Bipolar
• Yield Analysis
• Using mask design tools

13: Future of the processing
• Problems in submicron technology and Micromachining/sensors as a new fabrication area.
• Summary of main course points.
Electronics Industry
World’s Largest Manufacture

• Largest manufacturing industry in the world
Semiconductor fabrication equipment reached $US60 Billion/year (2018)
Transistor Inventors

- Bardeen, Brattain and Schockley at Bell Labs 1947 invented the first Transistor (bipolar point contact)
Transistor Inventors

- First planer transistor was invented by Jean Hoerni at Fairchild 1959

- Starting in January 1959, Hoerni worked on the planar process (for a PNP transistor, and then an NPN transistor)
- Hoerni made the first planar transistor in March 1959
- Decision to invest significant resources in the development of the planar
  - Much improved reliability and performance
  - Hoerni’s showmanship
  - Autonetics and the demands of military computing (Minuteman)
  - Competitive pressures (Rheem Semiconductor)
Integrated Circuits (ICs)

- A monolithic (single substrate) collection of devices
- First proposed by G. W. Drummer, UK 1952
- First produced by Jack Kilby of Texas Instruments 1958, he Received Nobel Prize in 2000 for microchip development

The first integrated circuit, invented in 1958 by Jack St. Clair Kilby of Texas Instruments, combined all the basic circuit elements in a single piece of germanium less than half an inch long (horizontal bar). The device was held together by glue, with gold wires providing interconnections.
Integrated Circuits (ICs)

- First Silicon IC produced by Robert Noyce of Fairchild 1959
Miniaturization is manifest in this comparison between an electromechanical switch, circa 1957, and a recent chip containing 16 million bits of memory (right). Progress appears in these snapshots (counterclockwise): Bell Laboratories' first transistor (1948); canned transistors (1958); salt-size transistors (1964); 2,000-bit chip (1973); boards with 185,000 circuits and 2.3 megabits of memory apiece (1985); and a 64-megabit memory chip (1992).
Transistors Overview

Introduction

 pn junctions are examples of 2 terminal 1 junction devices. There is one interface (junction) between the two components (can be same or different materials). A transistor is an example of a 3 terminal 2 junction device. The name transistor is derived from the term transfer resistance. The current (voltage) through two terminals is controlled by the current (voltage) through another pair of terminals. Thus, a transistor essentially acts as a switch. Another feature of the transistor is the ability to amplify a signal between one pair of terminals by using an input signal at another pair of terminals. Thus, a transistor can also act as an amplifier. A pn junction, on the other hand acts as a rectifier i.e. conducts in only one direction.

Bipolar junction transistor

A bipolar junction transistor (BJT) consists of three differently doped regions. These can have the configuration of npn or pnp and the various layers can either be parallel or perpendicular to the surface. Consider a pnp BJT, with three differently doped regions.

1. Emitter region - this is usually a heavily doped region (p⁺). The emitter ‘emits’ the carriers into the base.
2. **Base region** - this is a lightly doped $n$ region. The base region is also physically thin so that carriers can pass through with minimal recombination.

3. **Collector region** - this is a $p$ type region. The collector region has a larger width that the other two regions since charge is accumulated here from the base.

The symbols and nomenclature of the BJT transistor is shown in figure 2. Thus, a transistor consists of two $pn$ junctions, each with its own depletion region.

1. Emitter-base junction - since the emitter is usually heavily doped, the depletion region lies almost entirely in the base.

2. Base-collector junction - the depletion region at this junction is usually divided between base and collector, since they are comparably doped.

There are three different configurations in which the BJT can function - common base, common emitter, and common collector. The circuit connections are summarized in figure 3.
Figure 2: Symbols and nomenclature of a (a) npn and (b) pnp transistor. The BJT consists of three regions, emitter, base, and collector. The emitter and collector are usually of one type of doping, while the base is another doping type.

Figure 3: BJT transistor configurations - common (a) base, (b) emitter, and (c) collector configurations. Different configurations have different functionality in the circuit.
1 Common base (CB) configuration

In this configuration, the base is held common between the emitter and collector. This arrangement is summarized in figure 4. Looking at the circuit configuration, the emitter base junction is forward biased while the collected base junction is reverse biased. In a pnp transistor holes, which are the majority carriers in the emitter, are injected into the base. This constitutes the emitter current, $I_E$. These holes become minority carriers in the base, since it is doped $n$ type. Some of these holes recombine with the electrons in the base. Hence, electrons are injected into the base to compensate for that and this forms the base current, $I_B$. The base collector junction is reverse biased so that the holes that do not recombine in the base are swept into the collector and form the collector current, $I_C$. This current is due to hole drift since the flow is due to the applied electric field. The ratio of the collector current to the emitter current is called the current gain or the current transfer ratio ($\alpha$). Typical values of $\alpha$ are 0.99 - 0.999, i.e. only a small fraction is lost to recombination in the base. This is a consequence of the fact that the base region is physically thin and also lightly doped, so that the hole diffusion length is high. The total current in the circuit should be balanced, so that

$$I_E = I_C + I_B.$$  \[ \Rightarrow I_E \approx I_C \text{ since } I_B \text{ is very small} \]
The transistor action arises in the CB configuration when the collector-base voltage ($V_{CB}$) is higher than the emitter-base voltage ($V_{EB}$). This leads to a net power gain in the device. A BJT is an example of a current controlled device since the current in the output circuit is controlled by the current and voltage in the input circuit.

Figure 4: Summary of the common base BJT. (a) Schematic of the CB $p^+np$ BJT (b) Circuit diagram showing the connections. (c) Schematic of the currents and concentration gradients. (d) The various diffusion and drift currents in the transistor.
2 Common emitter (CE) configuration

The circuit diagram for the CE configuration is summarized in figure 5. In this configuration, the emitter-base junction is forward biased. The base current is the input current and the collector current is the output. Hence, the transistor acts as a amplifier since a small base current is amplified into a larger collector current. This amplification is given by the current transfer ratio ($\alpha$). If a time varying signal is applied to the base the amplified signal at the collector has the same time variation.

Figure 5: A common emitter configuration for the npn BJT. This configuration is used when a transistors is to be used as an amplifier. A small variation in base current is amplified at the collector, which acts as the out-put.
Transistors symbols and basic circuits

BJT is a current controlled device. For BJT configurations:

\[ \alpha = \frac{I_C}{I_E} \quad \text{and} \quad \beta = \frac{I_C}{I_B} \]

\[ I_C = \alpha I_E = \beta I_B \]

\[ \alpha = \frac{\beta}{\beta + 1} \quad \beta = \frac{\alpha}{1 - \alpha} \]

Common Base (CB) configuration for pnp transistor

Common Emitter (CB) configuration for npn transistor
Junction field effect transistor

In the BJT there are distinct emitter, base, and collector regions, forming 2 pn junctions. These regions exist even in the absence of an external bias, since they are created during the fabrication process. The device is current controlled, since carrier injection into the base and loss due to recombination decides the gain. In a field effect transistor (FET) current flow takes place through a channel in the device. The channel is either already fabricated in the device (junction FET) or is created by application of an external potential (metal oxide FET) and disappears when the bias is removed. The reason for calling these ‘field effect’ transistors is that the current flow depends on the width of the channel which is controlled by the external potential (electric field). Thus FETs are voltage controlled devices.

The basic structure of the JFET is shown in figure 6. The schematic picture of the device provides a greater understanding of the role of the channel. A JFET consists of 3 regions where electrical connections are made i.e. the source, drain, and gate. The channel provides the pathway for carrier transport from the source to the drain, while the gate bias (sign and magnitude)
affects the channel width and hence its resistance. By considering the behavior of the channel for different gate biases, it is possible to obtain the I-V characteristics of the JFET.

Figure 6: A junction field effect transistor (JFET). (a) Three dimensional representation of the JFET. (b) Cross section of the ideal JFET, showing the n-channel and the transistor symbol. (c) A practical implementation of the JFET. The electrical leads are on top and they are separated by using SiO as the insulator.
Consider a simple system where the gate is shorted with respect to the source. So $V_{GS}$ is zero and the drain is biased positively with respect to the source, so that $V_{DS} > 0$. For a $n$ channel, this leads to electrons flowing from the source to the drain (biasing would be reversed for a $p$ channel). The current flow in this scenario, with increasing $V_{DS}$, is summarized in figure 7. The $p$ regions (source and drain) in the transistors are heavily doped so that the depletion region falls in the $n$ side and the channel width is the region between the 2 depletion regions. In the bias condition shown in figure 7, the region between the source and the $p$ is forward biased while the region between the drain and $p$ is reverse biased. With increase in $V_{DS}$ the current flow in the channel increases but at the same time the channel starts to narrow near the drain side. Ultimately, beyond a certain value of $V_{DS}$, the channel is pinched off near the drain end. Hence, there is no increase in current, for a small increase in voltage, since there is injection of electrons in the pinched off region and these get swept into the drain. This is shown in the I-V characteristics of the JFET (with $V_{GS}$ zero) in figure 8. The current initially increases with $V_{GS}$ and then gets saturated after a certain voltage when pinch off occurs.
Figure 7: Carrier flow in a n channel with the gate shorted ($V_{GS} =0$). (a) With low $V_{DS}$ a current flows through the channel and increases with increasing $V_{DS}$ (b) With further increase in $V_{DS}$ the channel pinches off near the drain, since the drain gate junction is reverse biased. (c) After pinch-off, there is no further increase in current, reaching a saturation.
Figure 8: IV characteristics of the JFET for different $V_{GS}$. The current is highest when the gate is shorted. Applying a negative bias at the gate reduces the width of the channel and reduces the channel conductivity.
In a JFET device with the gate shorted, the channel width is determined by the dopant concentrations which also determines the voltage where pinch-off occurs. But by applying a potential to the gate it is possible to change the width of the channel. This is responsible for the transistor action, since the current across the two terminals (source and drain) is controlled by the voltage across two other terminals (source and gate). In a $n$ channel JFET if $V_{GS} > 0$ then the channel width will slightly increase but device modulation is not achieved (current control does not happen). On the other hand, if the gate is biased negatively with respect to the source, $V_{GS} < 0$, the channel width is reduced so that pinch off occurs earlier and the voltage where pinch-off occurs is determined the magnitude of $V_{GS}$. The channel behavior for a negatively biased gate is summarized in figure 9.

![Diagram](image)

**Figure 9:** Carrier flow with the gate negatively biased with respect to the source. (a) No $V_{DS}$, $n$-channel is narrower than a shorted gate (b) With positive $V_{DS}$, current flows occurs with channel narrowing near the drain. (c) Pinch-off happens at high $V_{DS}$ (lower than that for $V_{GS} = 0$)
Thus, with increasing value of $V_{GS}$ (negatively biased), the $V_{DS}$ at which pinch-off occurs comes earlier and also the current through the channel decreases. This is reflected in the I-V characteristics plot, shown in figure 8. With increasingly negative $V_{GS}$, the channel current decreases. There is also a critical value of $V_{GS}$ where the pinch off occurs before the device is in operation. This happens when the depletion width becomes wide enough that the channel is completely destroyed. In this scenario, no current flows through the channel, except for small leakage current due to thermal generation of the channel, except for small leakage current due to thermal generation of carriers. This is shown in figure 10. The drain current ($I_D$) in the channel depends on the value of $V_{GS}$ (field effect) by the expression

$$I_{DS} = I_{DSS} \left[1 - \left(\frac{V_{GS}}{V_{GS \ (off)}}\right)\right]^2 \tag{1}$$

where $I_{DSS}$ is the drain current with the gate shorted and $V_{GS \ (off)}$ is the gate voltage when the channel is destroyed. This behavior is plotted in figure 11.
Figure 10: At large negative bias (when $V_{GS} = -V_P = V_{GS\text{(off)}}$) the channel is completely destroyed (closed). There is only a small leakage current, similar to the reverse saturation current in the pn junction.

Figure 11: Drain current vs. gate source voltage in a JFET. With increasingly negative $V_{GS}$, the drain current reduces until it becomes zero. Maximum current ($I_{DSS}$) is when the gate is shorted.
Metal oxide semiconductor FET

The metal oxide semiconductor FET (MOSFET) is a particular type of FET where the channel for carrier conduction is created by the applied electric field. In this way MOSFET is different from the JFET, where the channel is already present in the material, and the applied electric field is used to narrow the channel to achieve transistor action. To understand the formation of the channel, under the effect of the applied field, consider a parallel plate capacitor arrangement, involving two metals, as shown in figure 12. Metals have a high electron density (typically $10^{21}$ to $10^{22} \text{ cm}^{-3}$). Hence the charges reside on the surface with minimal field penetration into the bulk.

Figure 12: Parallel plate capacitors with two metals, separated by an insulator. (a) One metal plate has a net positive charge on the surface and the other has a net negative charge. (b) The excess charges reside on the surface and do not penetrate in the bulk.
Consider a situation when one of the metals is replaced by a $p$-type semiconductor. This scenario is shown in figure 13. The metal is connected to the positive terminal and the $p$ type semiconductor is connected to the negative terminal. So a net positive charge resides on the metal surface. To maintain charge neutrality, a net negative charge must reside on the semiconductor. But the charge density in a semiconductor is much smaller than a metal (typically $10^{16}$ to $10^{18} \text{ cm}^{-3}$), so that in the semiconductor the charge not only resides on the semiconductor but also penetrates to a certain depth within the bulk, as shown in figure 13(a). Given that it is a $p$ type semiconductor and the excess charges are electrons there is thus a lowering of the hole concentration at a region near the surface. This is called a **depletion region**. With increase in applied voltage, the positive charge on the metal increases and the width of the depletion region in the semiconductor increases. Correspondingly, the electron concentration on the surface of the semiconductor increases. There is a certain voltage, called **threshold voltage**, $V_{th}$, above which there forms a region near the semiconductor surface where the electron concentration is higher than the hole concentration. This is called the **inversion region**. A $n$ channel is then created near the surface of a $p$ type semiconductor by the application of external potential. The formation of the inversion region, is shown in figure 13(b). In the inversion region, $n > p$, while in the depletion region, $p > n$ but $p \ll N_A$. 
Figure 13: Metal insulator semiconductor setup. Because of the difference in charge density between the metal and semiconductor, charges penetrate into the bulk of the semiconductor creating (a) Depletion region (b) Inversion (n-channel) and depletion at higher voltages.
The basic structure of the MOSFET is shown in figure 14. The figure shows a \textit{npn} MOSFET with three electrical connections, source, drain and gate,

![MOSFET diagram](image)

Figure 14: MOSFET basic structure with device symbol. There is a source, gate, and drain. The source and drain are connected to heavily doped \textit{n+} regions. The gate is separated from the \textit{p} semiconductor by an insulator and is used to form the \textit{n}-channel

similar to a JFET. This structure is called an \textit{enhancement MOSFET}. The bulk of the semiconductor is \textit{p} type with two heavily doped \textit{n+} regions near the source and drain. Thus, two \textit{pn+} junctions are formed, with the depletion region lying mostly in the \textit{p} side. The gate is usually made of metal or more recently, heavily doped poly-Si (with high electrical conductivity) and it is separated from the semiconductor by an insulator. The most common insulator is SiO\textsubscript{2}, which is the reason for the name \textit{metal-oxide-semiconductor}, though high \textit{k} dielectrics based on Hafnium, have replaced the simple silicon oxide. Electrical connections are made to the source, drain, and gate at different biases similar to the JFET.
4.1 MOSFET I-V characteristics

The I-V characteristics of the MOSFET is summarized in figure 15. In a npn MOSFET, the gate is biased positive with respect to the source ($V_{GS} > 0$). This reverse bias causes electrons to accumulate at the the $p$-type semiconductor oxide interface. Below the threshold voltage for inversion ($V_{th}$), there is no $n$-channel created and any current is due to thermally generated carriers and is negligible. When the gate voltage exceeds $V_{th}$, an $n$-channel is created. With the drain is biased positive with respect to the source ($V_{DS} > 0$), electrons flow from source to drain, through the $n$-channel. With increasing $V_{DS}$, given that the drain is reverse biased with respect to the $p$-type semiconductor, similar to the JFET, pinch-off occurs near the drain and the current is saturated. The typical I-V characteristics is shown in figure 16.

The graph is similar to that of the JFET, shown in figure 8. The difference lines in the behavior by changing the gate source voltage. In the JFET, the channel already exists, and the role of $V_{GS}$ is to narrow the channel and limit conduction. In the MOSFET the channel is created by $V_{GS}$ and its role is to increase conduction (below pinch off). Both JFET and MOSFET are voltage controlled devices. The gate voltage acts as a switch to turn on and off the device, providing the transistor action.
Figure 15: MOSFET I-V characteristics. (a) Below the threshold voltage, there is only an depletion region and no current at any $V_{DS}$. (b) When inversion is achieved (by increasing $V_{GS}$) an n-channel is created and current increases with applied $V_{DS}$.(c) After a certain point ($V_{DS(sat)}$), pinch-off occurs because voltage difference between gate and drain decrease → reducing inversion layer at B. (d) After pinch-off the current reaches a saturation
Figure 16: (a) MOSFET I-V characteristics, $I_D$ vs. $V_{DS}$ for varying gate voltages, $V_{GS}$ and (b) $I_{DS}$ vs. $V_{GS}$ for a given $V_{DS}$. In JFET, the applied gate voltage narrows the channel for conduction while in MOSFET, the applied gate voltage makes the channel wider.
Simple MosFet Transistor

- Need to create a isolated gate between source & drain
- Originally metal gate, now all polygate

The MOS transistor. (a) Diagram of an MOS transistor, showing gate, gate oxide, source, and drain. (b) Symbol for an $n$-channel MOS transistor. (c) Symbol for a $p$-channel MOS transistor.
Cross-section of a practical NMOS transistor.
MOSFET Threshold and Low Drain voltage

- When gate exceed threshold \((V_G >> V_T)\)
- Now channel filled with electrons: resistance reduced
- Note: this is called an enhancement mode FET
- Positive drain voltage causes carrier flow
- Get linear behaviour: called Triode or Linear region
- Higher gate voltage, more inversion, more carriers
  lower resistance and higher current flow
- As Drain voltage increase current flow
  causes voltage drop in channel
- Larger drain depletion region (more reverse biased)
- But carriers near drain decrease until get pinchoff
- Pinchoff or saturation voltage \(V_{Dsat}\)
Figure  Device cross section in (a) triode region, (b) onset of saturation, and (c) beyond saturation.
Increasing Density of Devices

- Growth with time - Transistors numbers/Chip
- Increase by 5000x in 15 years
- More value per chip

Microprocessor Transistor Counts 1971-2011 & Moore’s Law

curve shows transistor count doubling every two years
Moore's Law

- Moore's laws show industrial trends with time
- Intel co-founder Gordon Moore noticed in 1964
- Number of transistors doubled every 12 months while price kept unchanged
- Slowed down in the 1980s to every 18 months
- Amazingly still correct, likely to keep until 2010.
Transistor (MOSFET) Dimensions

- Transistor scale shrinkages
- Width of device, depth of device in Silicon, and thickness of critical films
## Road Map Semiconductor Industry

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<td>Transistors/cm²</td>
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**ASIC** = application-specific integrated circuit
## IC Scales

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<th>Abbreviation</th>
<th>Number of devices on a chip</th>
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<td>Super Large Scale Integration</td>
<td>SLSI</td>
<td>over 1,000,000,000,000</td>
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Semiconductors

- Conductors (e.g., copper/aluminum) have very low resistance.
- Insulators have very high resistance.
- Semiconductors have moderately high resistances, making them modifiable to lower values.
- A wire 1 mm square by 1 m long has 300,000 ohms resistance: native silicon.
- 0.1% impurity decreases the wire resistance by $3 \times 10^8 \times X$ to 0.001 ohms.
- Electrons are more tightly bound than metals.
- But much looser than insulators.
- Crystal structure: diamond-like tetrahedral (each atom bonded to 4 others).
- Semi shiny.
- Mono semiconductors: Column 4 in the periodic table. Examples include Germanium, Silicon, Diamond, and Grey Tin.
- Covalent bonding: sharing of electrons between two atoms.
- N-type dopants, from column V: add extra electrons (negative charges).
- P-type dopants, from column III: create holes (act as mobile positive charges).
**Binary and Ternary Semiconductor**

- Mono semiconductors: Column 4 in the periodic table:
- If average 4 electrons/atom get similar materials
- Covalent bonding: sharing of electrons between two atoms
- Binary semiconductors:
  - mixture of two elements that average 4 outer electrons.
  - eg. III-V materials
  - (GaAs: Gallium Arsenide, InP: Indium Phosphide),
  - or II-VI materials
  - (CdS: Cadmium Sulphide, HgTe: Mercury Telluride).
- NOTE: not all combinations are semiconductors
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<td>0.67</td>
<td>1.11</td>
<td>1.40</td>
</tr>
<tr>
<td>$n_i$ (cm$^{-3}$)</td>
<td>2.4 x 10$^{13}$</td>
<td>1.45 x 10$^{10}$</td>
<td>9 x 10$^{6}$</td>
</tr>
<tr>
<td>Intrinsic lattice mobilities (cm$^2$ V$^{-1}$ sec$^{-1}$)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Electrons</td>
<td>3900</td>
<td>1350</td>
<td>8600</td>
</tr>
<tr>
<td>Holes</td>
<td>1900</td>
<td>480</td>
<td>250</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>16.3</td>
<td>11.7</td>
<td>12</td>
</tr>
<tr>
<td>Melting point (°C)</td>
<td>937</td>
<td>1415</td>
<td>1238</td>
</tr>
<tr>
<td>Vapor pressure (torr)</td>
<td>10$^{-7}$ (@ 880°C)</td>
<td>10$^{-7}$ (@ 1050°C)</td>
<td>1 (@ 1050°C)</td>
</tr>
<tr>
<td>Specific heat (J g$^{-1}$ °C$^{-1}$)</td>
<td>0.31</td>
<td>0.7</td>
<td>0.35</td>
</tr>
<tr>
<td>Thermal conductivity (W cm$^{-1}$ °C$^{-1}$)</td>
<td>0.6</td>
<td>1.5</td>
<td>0.81</td>
</tr>
<tr>
<td>Linear coefficient of thermal expansion (ppm)</td>
<td>5.8</td>
<td>2.5</td>
<td>5.9</td>
</tr>
</tbody>
</table>
Crystal Structure

- Most semiconductor crystal structure: diamond like tetrahedral, each atom bonded to 4 others
- Binary compounds follows similar tetraheadral. However each atom hooked to both types Binary crystal structure called Zinc Blende (ZnS)

Diamond or zincblend: Two interpenetrating FCC’s
Miller Indexes and Crystal Planes

- Miller Indices are basic description of crystal plane
- Used to denote orientation of crystals

**Miller Index**

- Find intercept of plane on crystal axis
- Express intercepts as 3 integers
- Take r reciprocal of 3 integers
- Miller is smallest set of integers h, k, l having same ratio as reciprocals
- h for x axis, k for y, l for z
- eg. if intercepts at 4, 3, 2 → then reciprocal are 1/4, 1/3, 1/2
  → h = 3, k = 4, l = 6 (base of 12 in this case) → the plane is (346)
- For a plane show ( h k l )
- Direction is [ h k l ]

Fig. Miller indices of some important planes in a cubic crystal.
Crystal Planes and Wafers

- Wafers (thin slices of silicon) has specific planes
- Planes are that of the wafer surface
- Flats on wafers tell you the doping type of the wafer (n- or p-type) and the orientation of the wafer: \{100\} or \{111\}
Basic Process Steps in Microfabrication

• Design of Circuit (by computers) → rectile or mask
• Clean Wafer
• Deposit or grow layer of film (oxide film)
• "spin" on photosensitive material: photoresist
• Definition: Make pattern with Photolithography
• Develop photoimage (3D structure of photoresist).
• Etch away unwanted material
• Remove definition mask
• Sometimes other thermal or doping processes
• Repeat 7-20 times to defines layers as process requires
Basic Process Steps in Microfabrication

1. Prepared silicon wafer
2. Projected light
3. Patterns are projected repeatedly onto wafer
4. Areas unprotected by photoresist are etched by gases
5. Ions shower the etched areas, doping them
6. Similar cycle is repeated to lay down metal links between transistors

Metal connector

Photoresist
Silicon dioxide layer
Silicon substrate
Basic Process Steps in Microfabrication: Single Layer

Fig. Drawings of wafer through the various steps of the photolithographic process. (a) Substrate covered with silicon dioxide barrier layer; (b) positive photoresist applied to the surface of the wafer; (c) mask in close proximity to the surface of the resist-covered wafer; (d) substrate following resist exposure and development; (e) substrate following etching of the silicon dioxide layer; (f) oxide barrier on wafer surface after resist removal; (g) view of substrate with silicon dioxide pattern on the surface.
### Simple MOS Process

<table>
<thead>
<tr>
<th>Cross Section</th>
<th>Step</th>
<th>Operation</th>
<th>Name/Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>Layering</td>
<td>Field Oxide</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Patterning</td>
<td>Source/drain holes</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>Doping Layering</td>
<td>N-type doping and reoxidation of source/drain</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>Patterning</td>
<td>Gate region is formed</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>Layering</td>
<td>Gate oxide is grown</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>Patterning</td>
<td>Contact holes are patterned into source/drain regions</td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>Layering</td>
<td>Conducting metal layer is deposited</td>
</tr>
<tr>
<td></td>
<td>8</td>
<td>Patterning</td>
<td>Metal layer is patterned</td>
</tr>
<tr>
<td></td>
<td>9</td>
<td>Heat Treatment</td>
<td>Metal is alloyed to layer</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>Layering</td>
<td>Protective passivation layer is deposited</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>Patterning</td>
<td>Passivation layer is removed over metal pads</td>
</tr>
</tbody>
</table>

Figure 5.17 Formation of metal gate MOS transistor.
Contamination Control

• The most important aspect of microfabrication is control of dirt
• Processes killed by very small contaminants
Figure 1: Scanning electron micrograph (SEM) of an IC circa mid-1980s. The visible lines correspond to metal wires connecting the transistors.
Particle Sizes in Air

**FIGURE**

**PARTICLE SIZE DISTRIBUTION OF ATMOSPHERIC AIR**
(at a concentration of 69 Micrograms per Cubic Meter or .03 Grains per 1000 Cubic Feet)
For Typical Day

<table>
<thead>
<tr>
<th>PARTICLE SIZE (MICRONS)</th>
<th>AVERAGE QUANTITY PER CUBIC FOOT</th>
<th>PERCENT BY COUNT</th>
<th>PERCENT BY WEIGHT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.01 - 0.02</td>
<td>173,929,613</td>
<td>7.28%</td>
<td>-</td>
</tr>
<tr>
<td>0.02 - 0.05</td>
<td>338,577,845</td>
<td>14.17</td>
<td>0.02%</td>
</tr>
<tr>
<td>0.05 - 0.10</td>
<td>395,213,491</td>
<td>16.54</td>
<td>0.18</td>
</tr>
<tr>
<td>0.10 - 0.22</td>
<td>906,959,672</td>
<td>37.95</td>
<td>4.20</td>
</tr>
<tr>
<td>0.22 - 0.46</td>
<td>501,288,728</td>
<td>20.98</td>
<td>23.22</td>
</tr>
<tr>
<td>0.46 - 1.00</td>
<td>69,890,564</td>
<td>2.92</td>
<td>32.38</td>
</tr>
<tr>
<td>1.00 - 2.15</td>
<td>3,801,973</td>
<td>0.16</td>
<td>17.60</td>
</tr>
<tr>
<td>2.15 - 4.64</td>
<td>212,705</td>
<td>-</td>
<td>9.85</td>
</tr>
<tr>
<td>4.64 - 10.00</td>
<td>15,235</td>
<td>-</td>
<td>7.06</td>
</tr>
<tr>
<td>10.00 - 21.54</td>
<td>645</td>
<td>-</td>
<td>2.98</td>
</tr>
<tr>
<td>21.54 +</td>
<td>28</td>
<td>-</td>
<td>2.51</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>2,389,890,499</strong></td>
<td><strong>100.00%</strong></td>
<td><strong>100.00%</strong></td>
</tr>
</tbody>
</table>

Source: American Air Filter Research Laboratories
PARTICLE EMISSION FROM HUMAN ACTIVITY
(without cleanroom gowning isolation)

<table>
<thead>
<tr>
<th>Activity</th>
<th>Particles Emitted</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standing or Sitting - No Movement</td>
<td>100,000</td>
</tr>
<tr>
<td>Sitting - Light Head, Hand and Arm Movement</td>
<td>500,000</td>
</tr>
<tr>
<td>Sitting - Average Body and Arm Movement, Toe Tapping</td>
<td>1,000,000</td>
</tr>
<tr>
<td>Changing Position - Sitting to Standing</td>
<td>2,500,000</td>
</tr>
<tr>
<td>Slow Walking - 2.0 MPH</td>
<td>5,000,000</td>
</tr>
<tr>
<td>Average Walking - 3.57 MPH</td>
<td>7,500,000</td>
</tr>
<tr>
<td>Fast Walking - 5.0 MPH</td>
<td>10,000,000</td>
</tr>
<tr>
<td>Calisthenics</td>
<td>15,000,000 to 30,000,000</td>
</tr>
</tbody>
</table>
Clean Room Class Numbers
• Class = number of 0.5 micron particles/cu. ft.
• Modest clean room Class 1000
• State of art Class 1

Clean Room Garments
• For class 1000 cover most of body
• Class 100 - 10 must cover much of face
• Class 10 - 1 full face masks and breather filters
Basic Clean Room Layout

- Clean air from HEPA filters
- HEPA High Efficiency Particle Attenuators
- Call Laminar flow: means air does not have turbulence
- Air blows down from roof, and comes out from the bottom

Figure Cross section of clean-room tunnel.

Figure Cross section of laminar flow clean room. (Courtesy of Semiconductor International.)
Clean Room Building

- Clean room suspended within the building
- Vibration isolated from outside
HEPA Filters: High Efficiency Particle Attenuators

- HEPA filters very simple in concept: just folded aluminum foil and paper
- Air forced by foil to flow through many layers of filter
- As particles absorbed by filter, the air gets better, but air pressure drop rises
- Energy required to push the air through the HEPA filter area is

\[ E = \nu_a P \quad \text{W/m}^2 \]

\( \nu_a = \text{air velocity (m/s)}, \ P = \text{pressure drop (Pa)} \)
Deionized Water

- Water contamination as important as air
- Use Deionized (DI) water systems
- Removes heavy elements and biologicals
## Deionized Water

<table>
<thead>
<tr>
<th>Resistivity Ohms-cm 25°C</th>
<th>Dissolved Solids (ppm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>18,000,000</td>
<td>0.0277</td>
</tr>
<tr>
<td>15,000,000</td>
<td>0.0333</td>
</tr>
<tr>
<td>10,000,000</td>
<td>0.0500</td>
</tr>
<tr>
<td>1,000,000</td>
<td>0.500</td>
</tr>
<tr>
<td>100,000</td>
<td>5.00</td>
</tr>
<tr>
<td>10,000</td>
<td>50.00</td>
</tr>
</tbody>
</table>

Figure: Resistivity of water versus concentration of dissolved solids.
Specifications for Clean Room Utilities

- Air, Water, Chemicals, Gases are common utilities
- All must meet specifications listed

<table>
<thead>
<tr>
<th>SOURCE</th>
<th>SPECIFICATION</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Air</strong></td>
<td></td>
</tr>
<tr>
<td>Particulates</td>
<td>LSI Class 100 @ 0.5 micron</td>
</tr>
<tr>
<td></td>
<td>VLSI Class 10 @ 0.3 micron</td>
</tr>
<tr>
<td>Humidity</td>
<td>15-50%</td>
</tr>
<tr>
<td>Temperature</td>
<td>68-74°F</td>
</tr>
<tr>
<td>Photochemical Smog</td>
<td>2 pphm (parts per hundred million)</td>
</tr>
<tr>
<td><strong>Deionized Water</strong></td>
<td></td>
</tr>
<tr>
<td>Resistivity</td>
<td>15-18 meg Ω cm</td>
</tr>
<tr>
<td>Particulate</td>
<td>Less than 100 particulates per centiliter after 0.5 micron filtration</td>
</tr>
<tr>
<td>Bacteria</td>
<td>Less than 100 colonies per ml sample after 0.5 micron filtration</td>
</tr>
<tr>
<td><strong>Chemicals</strong></td>
<td></td>
</tr>
<tr>
<td>Metallic Impurities</td>
<td>Less than 1 ppm</td>
</tr>
<tr>
<td>Filtration</td>
<td>To 0.2 micron</td>
</tr>
<tr>
<td><strong>Gases</strong></td>
<td></td>
</tr>
<tr>
<td>Purity</td>
<td>Greater than 99.9%</td>
</tr>
<tr>
<td>Water Vapor</td>
<td>Less than 5 ppm</td>
</tr>
<tr>
<td>Filtration</td>
<td>To 0.3 micron</td>
</tr>
<tr>
<td><strong>Static Charge</strong></td>
<td>Less than 50 volts</td>
</tr>
</tbody>
</table>

Figure: Summary of clean-room requirements.

Figure: Sources of particulate contamination. This analysis, shown at SEMI Forecast by Dr. C. Rinn Cleavelin, Texas Instruments, revealed equipment-generated particles as the top enemy in 1985. (Courtesy of Semiconductor Equipment and Materials Institute.)
Silicon Wafers: Basics

- Silicon Wafers Basic processing unit
- 100, 150, 200, 300, 450 mm disk, 0.5-0.8 mm thick
- Current industrial standard 300 mm (12 inches)
- Most research labs uses 100, 150 mm wafers
- Typical process 25 - 1000 wafers/run
- Each wafer: 100 - 1000's of microchips (die)
- Wafer cost $10's - $100's
- 200 mm wafer weight 0.040 Kg
- Typical processing costs $1200/wafer (200 mm)
- Typical processed wafer value $11,000
  (all products, modest yield)
- Value/Mass of processed wafer $275,000/Kg
Production of Silicon Wafers

- Silicon starts as sand quartzite
- Most silicon used now is solar cell industry – lower grade
- China dominates polycrystalline & solar grade 4.6 Megatonnes (2010)

Conversion of Raw Sand into Metallurgical Grade Silicon

Fig. Process sequence from starting material to polished wafer.
Step 1: Metallurgical Grade Silicon (MGS): 98% pure
• Start with white beach sand (quartzite or SiO₂)
• Use electric arc to melt in mixture of coal coke, wood at 2000 °C; **Coke** is a fuel with a high carbon content and few impurities, made by heating **coal** in the absence of air
• Carbon removes impurities: molten Si drawn from bottom

- Overall reaction: $SiO_2 (s) + 2C (s) \rightarrow Si (l) + 2CO (g)$
- Takes considerable power: 12-14 KWh/Kg of Si

<table>
<thead>
<tr>
<th>Element</th>
<th>Concentration (ppm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al</td>
<td>1000-4350</td>
</tr>
<tr>
<td>B</td>
<td>40-60</td>
</tr>
<tr>
<td>Ca</td>
<td>245-500</td>
</tr>
<tr>
<td>Fe</td>
<td>1550-6500</td>
</tr>
<tr>
<td>P</td>
<td>20-50</td>
</tr>
<tr>
<td>Cu</td>
<td>15-45</td>
</tr>
</tbody>
</table>

Table: Impurities in MGS in parts per millions (ppm) after the submerged arc electrode process.

Metallurgical grade silicon (poly crystalline)

Submerged electrode arc furnace for metallic silicon production

(1) Clean enough for metallurgical applications
(2) Not single crystal → Polycrystalline
(3) Not pure enough for electronic applications
Step 2: Metallurgical Grade Silicon Chemical Purification
• Convert MGS solid powder to trichlorosilane (SiHCl$_3$) by reacting with anhydrous hydrogen chloride (AHCL) at 300 °C

\[
Si (s) + 3HCl (g) \rightarrow SiHCl_3 (g) + H_2 (g)
\]

• Chlorine reacts with impurities to give material like AlCl$_3$, etc.
• Trichlorosilane (SiHCl$_3$) boils at 31.8 °C

Step 3: Distill Trichlorosilane
• Impurities reduce to parts per billion (ppb)
• Reduced by about 10$^8$ from original values

Step 4: Silicon Chemical Vapour Deposition
• Gaseous trichlorosilane (SiHCl$_3$) reacted with Hydrogen

\[
SiHCl_3 + 2H_2 \rightarrow 2Si + 6HCl
\]

• Si deposits by CVD out on rods with large crystals: Polycrystalline
• Result Electronic Grade Silicon (EGS)
• Called the Siemens process
• Total production 3 million Kg 1985
Table: Impurities in EGS, after purification from MGS. Compared to table before, the concentration levels of the metals have dropped to ppb levels.

<table>
<thead>
<tr>
<th>Element</th>
<th>Concentration (ppb)</th>
</tr>
</thead>
<tbody>
<tr>
<td>As</td>
<td>&lt;0.001</td>
</tr>
<tr>
<td>Sb</td>
<td>&lt;0.001</td>
</tr>
<tr>
<td>B</td>
<td>&lt;0.1</td>
</tr>
<tr>
<td>C</td>
<td>100-1000</td>
</tr>
<tr>
<td>Cu</td>
<td>0.1</td>
</tr>
<tr>
<td>Fe</td>
<td>0.1-1</td>
</tr>
<tr>
<td>O</td>
<td>100-400</td>
</tr>
<tr>
<td>P</td>
<td>&lt;0.3</td>
</tr>
</tbody>
</table>

EGS is (1) highly pure for electronic applications (2) polycrystalline
Czochralski Crystal Growth methods

- Czochralski (CZ) basic Silicon crystal growth method
- Melt Poly Si EGS at 1430 °C in quartz crucible
- Rotate crucible clockwise
- Bring counterclockwise rotating seed crystal to melt Si
- Slowly draw seed from melt
- Atoms of melt freeze out aligned with crystal planes of seed
Czochralski Crystal Growth

- As seed drawn from melt initially grow narrow neck
- Dislocations (incorrect crystal alignment stopped at neck)
- As slow rate of pull (withdrawal) crystal diameter grows to max
- Maintain constant rotate/pull rate for uniformity eg 20 cm/hr
- Ingots up to 200, 300 and 400 mm diameter now possible
- Limit is weight that can be held by seed end (tang)
- Bottom called the butt end
Movement of Impurities from Melt to Crystal

• To put dopants in wafer place impurity in melt
• Equilibrium concentration (solubility) different in solid, \( N_s \) than in liquid \( N_l \)
  (note solubilities often symbolized as \( C_s, C_l \))
• Segregation ratio fraction of liquid dopant in solid

\[
k = \frac{N_s}{N_l}
\]

• Also as crystal pulled, melt dopant concentration changes with pulled \( X \)
  (fraction of melt solidified) (\( X=0 \) at the seed end). The solid dopant concentration
  changes according to

\[
N_s = kN_{l0}(1 - X)^{[k-1]}
\]

\( N_{l0} \) is the initial dopant concentration in liquid.

• Thus dopant concentration changes along length of crystal
• Thus impurities & dopants differ in each wafer
• Hence measure each wafer resistivity is necessary
A Si crystal is to be grown by the Czochralski method, and it is desired that the ingot contain $5 \times 10^{15}$ arsenic atoms/cm$^3$.

(a) What concentration of arsenic atoms should the melt contain to give this impurity concentration in the crystal during the initial growth? For As in Si $k_d = 0.3$.

(b) If the initial load of Si is 4.0 kg, how many grams of arsenic should be added? The atomic weight of arsenic is 74.9.

Solution:

(a) Assume that $C_S = k_d C_L$ throughout the growth. Thus the initial concentration of As in melt should be

$$\frac{5 \times 10^{15}}{0.3} = 1.67 \times 10^{16} \text{ cm}^{-3}$$

(b) The As concentration is so small that the volume of melt can be calculated from the weight of Si. The density of Si is 2.33 g/cm$^3$.

Total volume of the melt = $\frac{4000 \text{ g}}{2.33 \text{ g/cm}^3} = 1717 \text{ cm}^3$.

Total number of As atoms = $1.67 \times 10^{16} \text{ cm}^{-3} \times 1717 \text{ cm}^3 = 2.87 \times 10^{19}$ As atoms.

1 mole As $\rightarrow$ 74.9 g

$2.87 \times 10^{19}$ As $\rightarrow$ ?? g

Total weight of As atoms to be used = $\frac{2.87 \times 10^{19} \text{ atoms} \times 74.9 \text{ g/mole}}{6.02 \times 10^{23} \text{ atoms/mole}} = 3.57 \text{ mg of As.}$
Float Zone Crystallization

- Float Zone (FZ) produces smaller wafers
- Start with polycrystalline Si rod (ingot)
- Touch rod to seed crystal
- Heat with moving Radio Frequency (RF) coil
- Melts road near coil
- Move melt front from seed crystal to end and back
- Leaves single crystal rod (ingot) behind

Comparison of CZ and FZ wafers
- FZ better impurity → higher resistivity, but smaller size
- Reason: FZ process move impurities to ends of rod
Rod (Ingots) Sawing

- Use diamond saws to cut Crystal rods
- Very thin blades
- Resulting slices called wafers
- Typical wafer about 0.5 -0.8 mm thick (100-450 mm wafers)
- Lose nearly half material in cutting
- Large gain poly Si square wafers used for solar cells
**Wafers Polishing**

- Wafers mechanically abrasive polished to reduce roughness
- Then chemical/mechanical polished
- Film thickness are 0.1 microns or smaller for devices
- Thus wafers polished to < 10 nm defects

**Wafer Polishing Process**

**Chemical Mechanical Planarization (CMP)**

During the polishing process, polishing pads and diamond liquid slurry are used to polish the wafer. The wafer is held in place by a vacuum carrier such that the backside of the wafer is exposed. The carrier and wafer are slowly brought into contact with a rotating platen, which is covered by a polishing pad. With a controlled downward force, we are able to carefully remove the damaged layers of the wafer, creating a stronger end product for the customer. When working with thin silicon, keeping it damage-free is a challenge. That's why we recommend wafer polishing to remove the micro-damage that can result from the backgrind process. Wafer polishing is both highly effective and safe.
Flats and Wafer types

- Flats are cut in the single crystal rods
- Allows wafers can to orientated and identified
- Primary flat largest: used to orientate wafer
- Secondary (minor) flat position varies with crystal type and orientation
- 300, 450 (and some 200) mm wafers use a notch for orientation
- Notch is 1 mm deep at <110> orientation for <100> wafers